

Implementation of level shifted MCPWM technique and OCFT capability in multilevel inverters

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Abstract: A five level single phase multilevel inverter is advanced in this paper which remarkably lessens the number of semiconductor devices used, particularly for large number of voltage levels along with open circuit fault tolerance capability. This topology is proposed by using MCPWM technique. When it comes to comparison with other topologies this topology has reduced number of devices. This topology resembles by some means with CHB (cascaded hybrid bridge). The topology is consist of two DC sources (each of $E_1=E_2=24V$) in such a way that the higher potential side of one DC source is connected to the lower potential side of another DC source and vice versa. In reduced device count multilevel inverters the redundant states are significantly lowered which influences the fault tolerant ability of multilevel inverters. This study has been done in order to convey fault tolerant quality to reduced device count multilevel inverters. In this paper the OCFT is based on ASSOF (any single switch open circuit fault). Therefore, an extra switch is added in order to overcome the fault. The overall topology is simulated and verified through calculated and experimental results using software.

Index Terms— Reduced device count MLI, open circuit fault tolerance, level shifted MCPWM, symmetrical.

I. INTRODUCTION

Multilevel inverters are extensively used for the high power DC to AC transformation applications since for years. Nowadays, MLI's are extensively contributing in industrial applications and providing solutions for high power applications. The advantages that MLI's are providing are, less dv/dt stresses, higher voltage Capability, high switching frequency and fault tolerant capability. Nevertheless, they are getting popularity in this era, but their large number of devices, high cost, Size, and control has restricted their penetration in the market [1]. The quality of multi-level inverter is intensified by enlarging the number of levels but enlarging number of levels in turn increases the number of DC inputs and switches which makes the overall system complicated and difficult to Implement [2]. Therefore, it is essential to lessen the number of device count for practical implementation [3]. In this research An inverter with reduced number of semiconductor devices and gate drive circuits is proposed.

Many researchers have worked on many topologies of inverters. Likewise, (flying capacitor, neutral point clamped and cascaded hybrid bridge) [4]. Among these topologies CHB has gain more interest and popularity Because of its

inherent advantages [5]. It has better harmonic distortion profile as compared to other topologies. The only drawback it has that for every h-bridge it requires separate DC input which increases the total number of devices and makes it complicated. For this reason a topology is proposed in this paper which uses reduced number of devices. This topology shows resemblance with CHB in some manner. A high switching frequency method is used in this technique [6].

The emergence of RDC MLI's nowadays is incredibly increasing. One of the major concern of RDC MLI 's is their reliability. An inverter must be capable of handling any problem or fault that is occurring [7]. There are two types of faults that usually occurs. Open Circuit fault and short circuit fault. The open circuit fault happens because of thermal cycling [8]. The short circuit fault happens because of overvoltage, wrong gate voltage, avalanche or due to high temperature [8]. These problems must be sorted out. This paper has worked on these problems and provides solution as well. Though, the study has been done on an open circuit fault of inverter. The OCFT capability of an inverter depends on the number of redundant states which in turn depends on the number of devices that are used [9]. This shows that an inverter with large number of semiconductor devices has more redundant states than an inverter with reduced devices. Therefore, in RDC MLI's the redundant states are low which effects their OCFT capability. In this research the fault tolerant capability of RDC MLI is Improved. For OCFT capability, an extra switch is imparted in this topology without increasing the number of devices.

This paper is divided into six sections. The working and operation of this technique is explained in the section II. The simulation is shown in section III. Results along with discussion are shown in section IV. The concluding remarks are narrated in section V. References are provided in section VI.

II. METHODOLOGY

A. Generalized form proposed RDC MLI

The composition of following topology is shown in fig 1. The operation and working of proposed technique is elucidated with the support of single phase five level inverter.

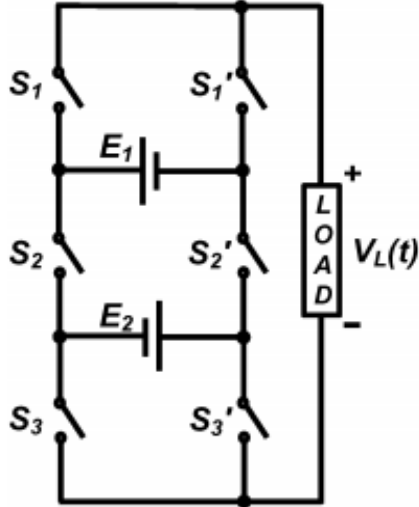


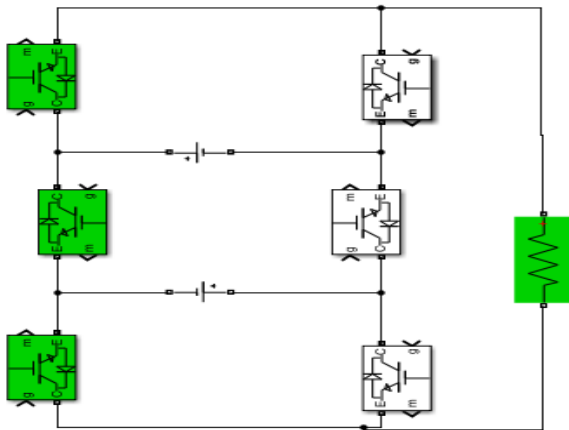
Fig. 1. General form of RDC MLI topology

B. Working rule

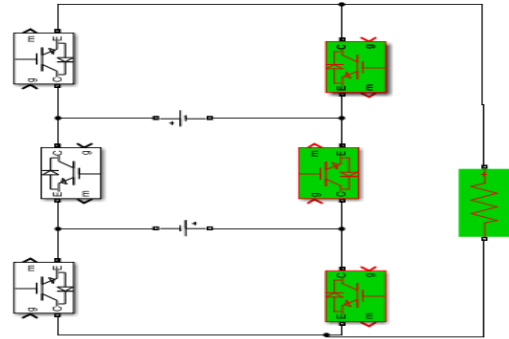
The topology is consist of two DC sources (each of $E_1=E_2=24V$) in such a way that the higher potential side of one DC source is connected to the lower potential side of another DC source and vice versa. The topology comprises of six switches that are complementary with one another. Both IGBT's and MOSFET's can be used in this technique. In this paper IGBT's are used. There are total eight switching modes. All of the modes are valid and combines to yield five levels (-2V, -V, 0V, 2V, V) at the output of inverter. The DC sources are assumed to be equal in this case whereas, practically they may differ.

C. Operating modes

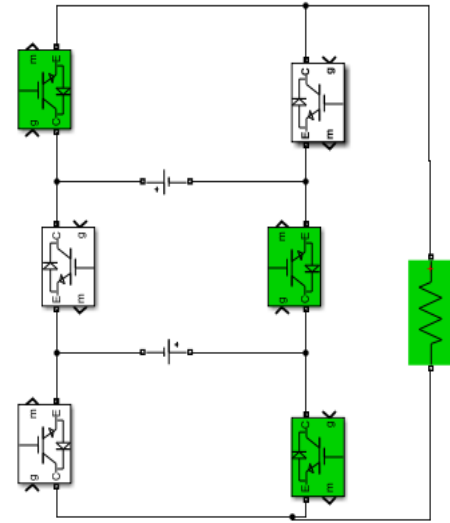
Operation 1



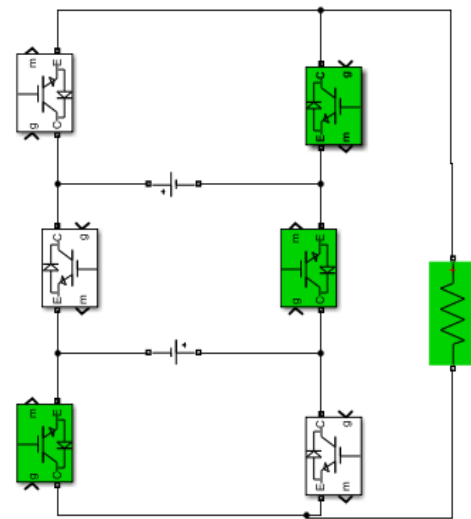
Operation 2



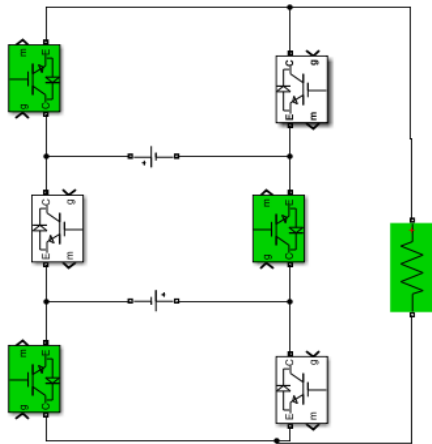
Operation 3



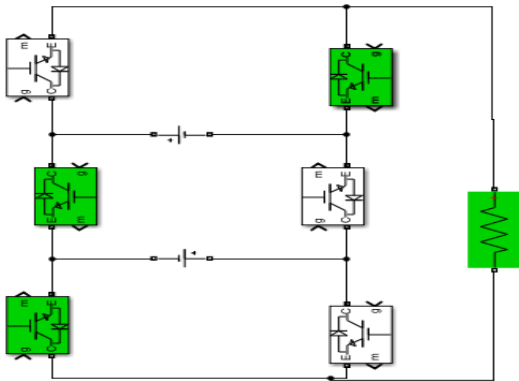
Operation 4



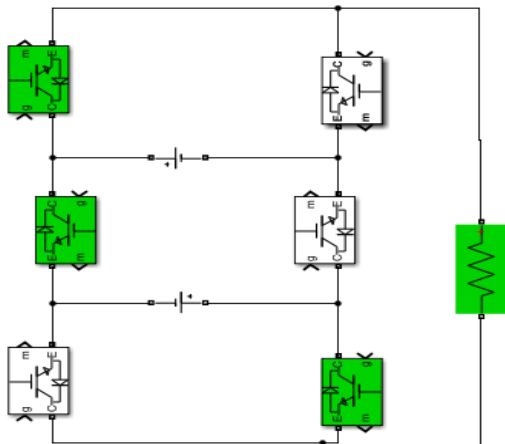
Operation 5



Operation 6



Operation 7



Operation 8

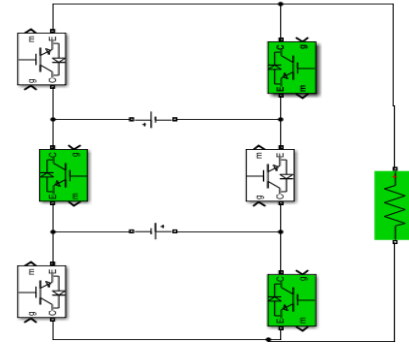


Fig.2. Valid operating modes for the proposed topology in fig.1

Table 1

Switching table for valid operating modes

S1	S2	S3	Output voltage
0	0	0	0V
1	1	1	0V
1	0	0	+V
0	0	1	+V
1	0	1	+2V
0	1	1	-V
1	1	0	-V
0	1	0	-2V

D. Modulation technique

For the proposed topology the MCPWM (multicarrier pulse width modulation) technique is used. This modulation technique has advantage of reducing total harmonic distortion and improves the output of multilevel inverter. It has high switching frequency. A recommended signal of 50hz is used for the comparison of carrier signals (each of 1khz frequency) and the acquired pulses are then used for the switching of semiconductor devices.

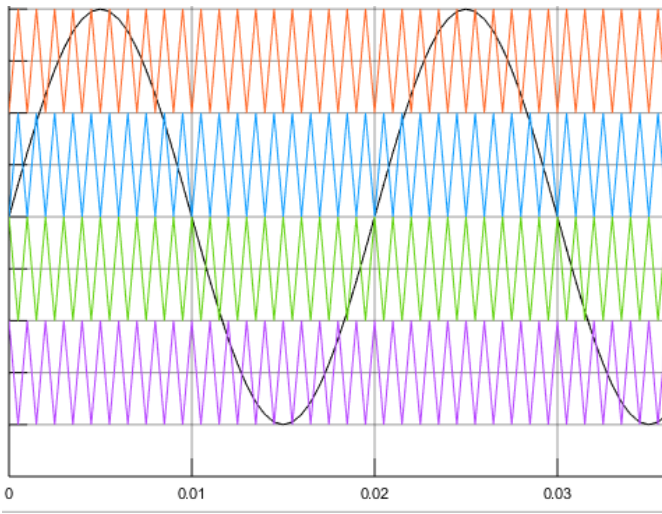


Fig.3. POD MCPWM technique

In POD technique the carriers above the axis are phase shifted with the carriers that are below the axis

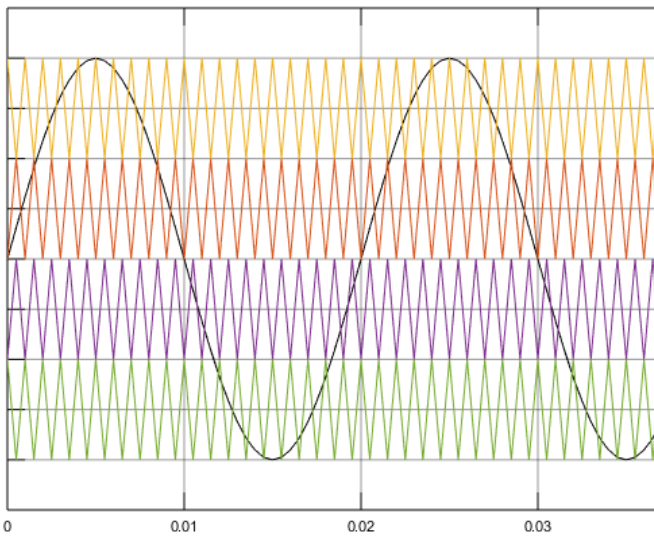


Fig.4. APOD MCPWM technique

In APOD technique the carriers above and below the axis all of them are phase shifted with each other

E. Open circuit fault tolerant capability:

For the reliability of RDC MLI, an open circuit fault tolerant capability is induced in this proposed topology. For the operation of OCFT capability an extra switch is imparted in the generalized structure which is shown in fig.1. Due to less redundant states the highest level cannot be achieved at the output of inverter during fault but inverter continues to operate at low levels when any single switch is disconnected from the circuit. When Any one of the six switches is opened, the

inverter continues to operate with the help of extra switch that is added and gives three level output. This research is carried out in case of any single switch stops working because usually not more than one switch fails at a time.

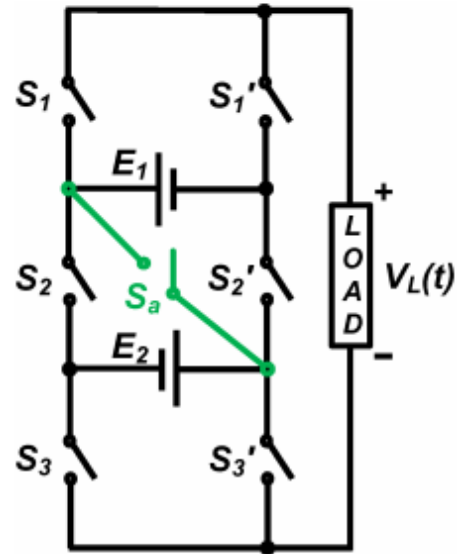


Fig.5. Modified RDC MLI with OCFT capability

Table 2

Obtainable states in case of any single switch failure

FAILED SWITCH	OBTAINABLE MODES	OUTPUT LEVELS
S1	2, 4,5, 8	Three levels
S2	2, 3, 4,7	Shut down
S3	2, 3, 6, 8	Three levels
S1'	1, 3, 6, 7	Three levels
S2'	1, 5, 6, 8	Shut down
S3'	1, 4, 5, 7	Three levels

From the table it is clearly shown that complete shutdown occurs when the switch S, S2' to operate. Therefore, desired level should be achieved in case switch S2 fails.

Table 3

Switching states when S2 fails after adding an extra switch 'Sa'

On state	Output voltage	Voltage level
S1, Sa, S3',S1',S2'	0Vdc	Three levels
S1',S2',S3',S1,Sa,S3	+Vdc	
S1',Sa, S3'	-Vdc	

Table 4

Switching states when S2' fails after adding an extra switch

ON STATE	OUTPUT VOLTAGE	VOLTAGE LEVEL
S1, S2,S3,S1,SA,S3'	0Vdc	Three levels
S1, SA, S3	+Vdc	
S1',SA,S3',S1,S2,S3'	-Vdc	

III. SIMULATION

The proposed topology is simulated through the MATLAB SOFTWARE. The two symmetric DC inputs are used (E1=E2=24V). IGBT's are used as switches in this topology. The positive cycles for output levels are obtained through the modes(1, 3, 4,7). The negative cycles for output levels are obtained through the modes (2, 6,, 7, 8). For the switching of all IGBT's a control circuit is also designed in software.

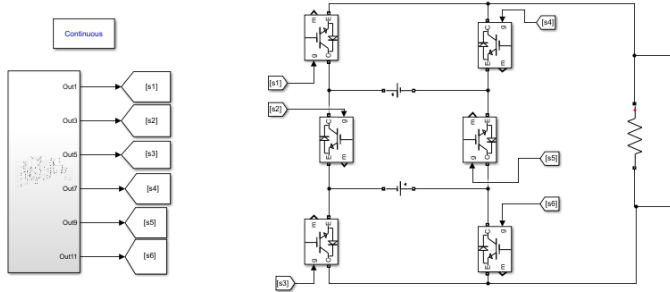


Fig.6. MATLAB simulation of proposed topology

IV. RESULTS AND DISCUSSION

The simulation of proposed RDC MLI topology is done on MATLAB software and the results are shown in fig.8. Both POD and APOD techniques are used to analyze the performance of output voltage and total harmonic distortions. Four triangular carriers are used, and sine wave is used as a reference signal.

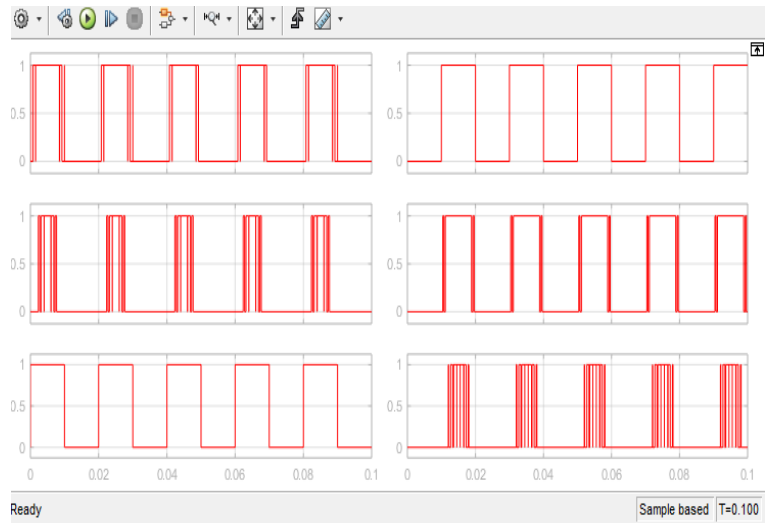


Fig.7. Switching pulse pattern for switching of IGBT's

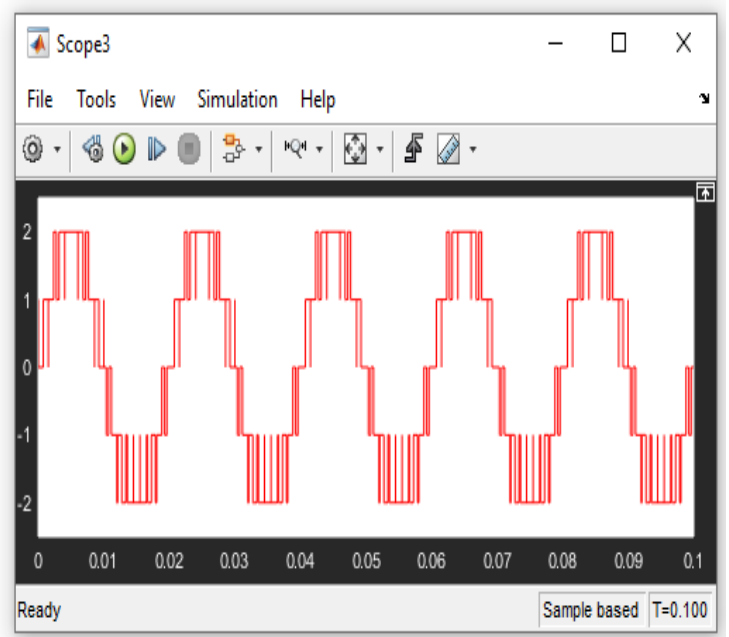


Fig.8. Five level output of proposed RDC MLI using APOD And POD technique

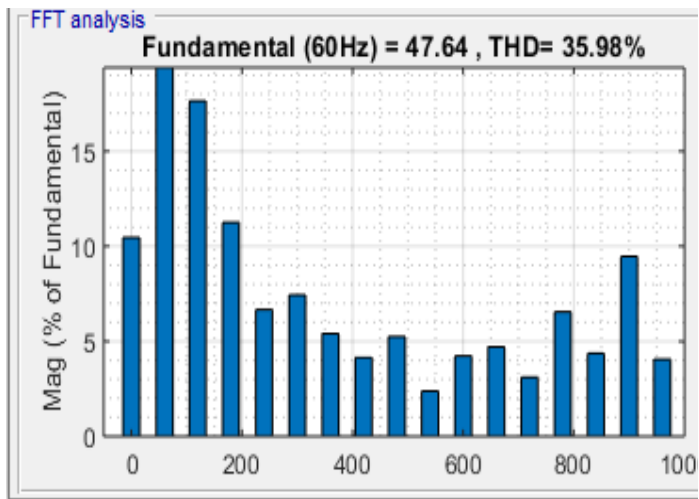


Fig.9. THD when APOD technique is used

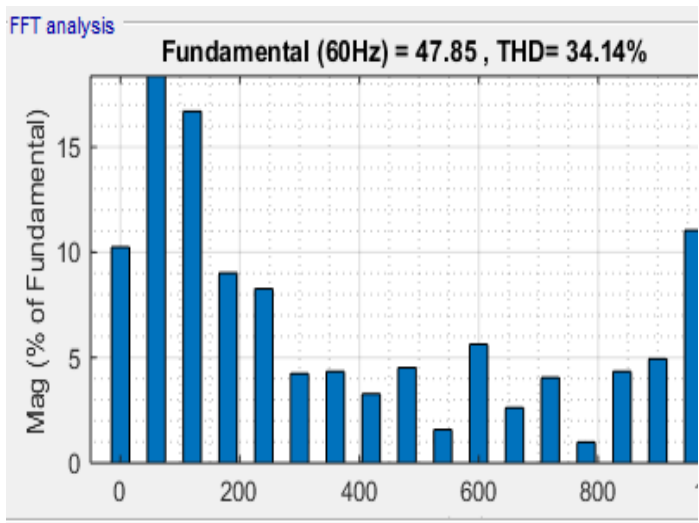


Fig.10. THD when POD technique is used

It can be observed from fig.9 and fig.10 that the proposed topology shows less harmonic distortion in POD technique than the APOD technique.

V. CONCLUSION

A reduced device count inverter with the help of single phase five level inverter has been proposed in this paper. The main motive was to reduce the number of semiconductors, gate drive circuits and to make system less complicated and more reliable. A remedy for fault tolerant operation was also proposed in this topology with the help of an extra imparted switch. When compared to other topologies (FC, NPC, CHB), the proposed topology has effectively reduced the number of devices and is more easily implemented. It is also concluded from the results that the proposed topology can satisfactorily operate in case any single switch fails. The proposed

topology has shown better harmonic performance using POD technique than APOD technique.

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