International Journal of Electrical Engineering & Emerging Technology, Vol. 03, No. 02, DEC 2020, pp 45-51

Design of Reduced Device Count Multilevel Inverter by Using Multicarrier PWM Techniques.

[a*]Arshad Ali Lashari, [b]Yaseen Ahmed Panhwar, [c]Shakir Ali Kalwar, [d]Touseef Ali Shahani, [e]Mushtaque Ali Dal, [f]Pirah Peerzada
Mehran University of Engineering and Technology Jamshoro, Pakistan
Corresponding author e-mail: (Arshad00123456@gmail.com)
[**Received on:** 15-11-2020 **Accepted on**: 30-11-2020 **Published on:** 08-12-2020]

Abstract: **The world is moving towards renewable power generation. In this regard solar PV panels are being widely adopted for power producing. Since an interface is always needed whenever there is mismatch between supply and load. Although conventionally inverters are available, but their output is not pure sinusoidal and contains certain harmonics. Multilevel inverters provide output waveform better than conventional inverter by producing number of levels of output voltage. But as the number of output levels are increased, the number of switching devices and voltage sources. This gap is filled by using reduced-device count MLI topologies. So RDC MLIs are trend in trend in the research era of power electronics. The beauty of PWM control makes it more attractive for an effective power conversion. In this project a 7-level RDC MLI is designed. The circuit contains separate parts for both level and polarity generation. The proper combination of logic gates is employed for generating the switching signals for 8 IGBTs from 6 high frequency carrier signals. The carriers have switching frequency of 1.5 kHz and reference sine wave is compared the signals are generated. This whole work is done on MATLAB- SIMULINK software.**

Index Terms **– Multicarrier PWM, Reduced Device Count Multilevel Inverter, Total Harmonic Distortion**

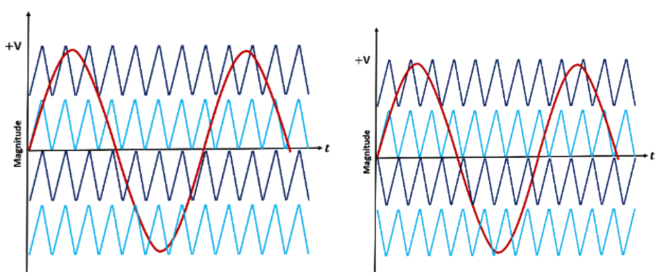
I. INTRODUCTION

Pulse width modulation (PWM) is the basis for the control in power electronics. Solid state devices used in power converters can be effectively driven by using these techniques. Vast majority of power electronic converters nowadays use these techniques, to convert currents and voltages from direct to alternating and vice versa. The aim of this research work is to design a reduced device count multilevel inverter by using multicarrier PWM techniques, with less harmonics, because harmonics cause the serious power quality issues. These are nothing but multiples of fundamental frequency. All complex waveforms other than sinusoidal waveform contain certain higher order harmonics. The second harmonic will be of frequency twice the supply frequency, third will be three times and so on. If the nature of complex waveform is possessing half wave symmetry, then the waveform will contain odd harmonics only. [1] This inverter uses asymmetric configuration of two voltage sources and eight switches to produce seven level output voltage. Multilevel inverters are being widely used for smooth and distortion free conversion of DC power into AC. As the number of levels increases, the number of devices i.e. switches and other electronic equipment also increases, which make the design too complex, bulky and uneconomical, for this a reduced device count multilevel inverter should be deigned to have effective conversion with less complexity. Multicarrier PWM techniques have been widely applied for the design of multilevel inverters, but when it comes to reduced device count, it becomes difficult to design a proper logic from the several available carriers and to provide those logics to the switches used in the circuit. Logic gates are simpler and easier to be used for this pulse generation purposes for IGBTs and MOSFETs etc. A Multilevel inverter is superior to two-level inverter in efficiency, performance and better harmonic spectrum. [2] But increasing number of levels tends to increase number of devices and gate drivers for switches, which make the overall design complex, bulky and uneconomical for the medium voltage applications. [3]. Therefore, reducing the number of devices without reducing the output voltage level is the key era of research in the field of power electronics. Increasing number of levels costs huge increase in number of devices used, which is the main disadvantage of multilevel inverter. Moreover In the conventional topologies of multilevel inverter dc voltage bus is not fully utilized, whereas the usage of dc bus voltage in the RDC MLI configurations normally gets doubled compared with the conventional one, therefore, the dc bus voltage can be reduced to the half of the voltage level in order to produce the same result as the traditional configuration. [4] This gives rise to the concept of RDC MLI. Multilevel inverters are being widely used for smooth and distortion free conversion of DC power into AC, as well as in high reliability drives. [6] RDC MLIs provide a design that significantly reduces number of switches, their gate drivers and other circuitry.[7] As compared to Neutral point clamped (NPC) and Flying capacitor (FC) multilevel inverters, the cascaded H-bridge is more attractive because of its simplicity in control as well as in modularity, CHB MLI requires less number of devices as compared to other two. [8] MLI with voltage sources of same voltage are termed as symmetric MLI, whereas those having different voltage source values are known as asymmetric MLI. [9] RDC MLIs producing less conduction losses, lesser size and better efficiency, which create its importance in low as well as medium power applications. [10] [11] [12] [13] [14] Moreover asymmetrical configurations provide better reduction in devices as compared to symmetric ones. [15] Thus economic optimization is obtained with the help of these RDC MLIs. [16] Thus this superiority along with significant reduction in dynamic losses make RDC MLIs current trend in the era of power electronic converters [17]. Use of active devices (switches) helps in reducing the number as well as size of the devise used in the respective MLI. [18]

II. MULTICARRIER PWM TECHNIQUES

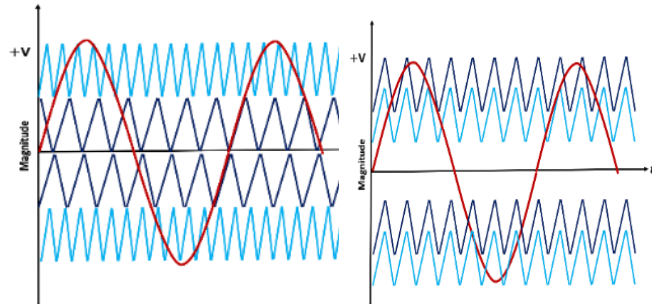
Multicarrier PWM techniques use multicarrier strategy for the operation. Triangular wave is taken as carrier wave and multiple triangular waves of high frequency are produced, which are then compared with the reference sine wave. And the multiple switching signals for multiple output levels are produced. Mainly the types of multicarrier PWM techniques employed widely in power electronic converters, differ from each other on the basis of respective carriers.

In PD multiple carriers PWM technique the number of carrier waves are produced. The number of carrier signals required for an N-level multilevel inverter will be (N-1) it means to design a 7-level multilevel inverter, 6 carrier signals will be required. In POD the triangular carrier waves above the x-axis have 180 ° phase shift as compared to those carrier signals which are below x-axis. The number of carrier signals in this technique to design a particular output level inverter are exactly same as in PD technique i.e. (N-1) carriers for N level output.



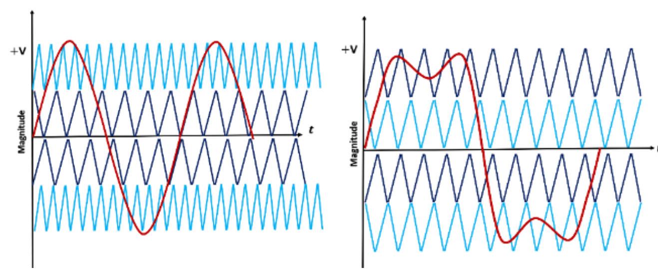
(a) (b)

In APOD MCPWM technique, each carrier above x-axis has 180° phase difference to its neighboring carrier. In CO MCPWM technique the high frequency carrier signals overlap each other. It is to be noted that signals will not intersect each other but the lower carrier moves in the area of the upward carrier.



(c) (d)

In VFC PWM technique all carriers above x-axis have same difference but different frequency. Similarly, all carriers below x-axis have same phase difference but different carrier frequency, but 180 ° out of phase difference with above x-axis carrier signals. In SFO MCPWM technique, there is little bit change in the sinusoidal signal, so when the inverter is operated in over modulation mode i.e. the inverter has maximum reference signal magnitude So at that time if one wants to operate the inverter around 80% modulation index, this PWM technique, can be employed in order to get maximum power and output voltage.



(e) (f)

Fig. 1. **(a)** Phase disposition MCPWM, **(b)** Phase opposition disposition MCPWM, **(c)** Alternate Phase opposition disposition, **(d)** Carrier Overlapping (CO) MCPWM, **(e)** Variable Frequency Carrier (VFC) MCPWM, **(f)** Switching frequency Optimal (SFO) MCPWM.

III. PROPOSED RDC-MLI

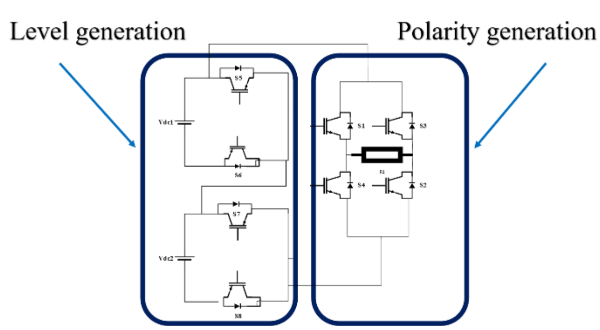


Fig. 2. Proposed RDC-MLI

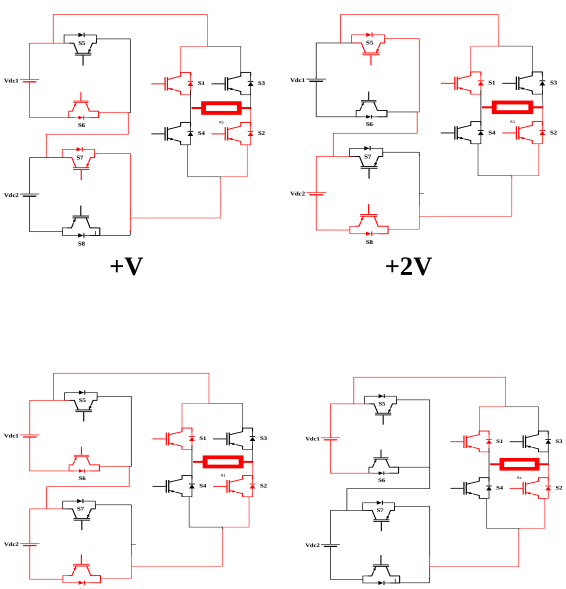
The experimental circuit contains separate part for the level and polarity generation, the level of the output voltage is generated as because of left portion, whose respective polarity is given by the full bridge. As shown in the figure switches S1, S2, S3 and S4 contribute to the polarity generation part, whereas the levels of the output voltage are being generated by the switches S5, S6, S7 and S8. The topology is asymmetric nature, because both voltage levels vdc1 and vdc2 have different voltages. The input voltage vdc1 has a value of 104V where as vdc2 is of 208 volts. Switches S1 and S2 conduct only for the positive half cycle of the output voltage, whereas S3 and S4 contribute when negative half cycle of the output voltage is generated. The switching table of all switches is given in Table I

Table I. Switching Table

LEVEL	S1	S2	S3	S4	S5	S6	S7	S8
0	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
+V	ON	ON	OFF	OFF	OFF	ON	ON	OFF
+2V	ON	ON	OFF	OFF	ON	OFF	OFF	ON
+3V	ON	ON	OFF	OFF	OFF	ON	OFF	ON
-V	OFF	OFF	ON	ON	OFF	ON	ON	OFF
-2V	OFF	OFF	ON	ON	ON	OFF	OFF	ON
-3V	OFF	OFF	ON	ON	OFF	ON	OFF	ON

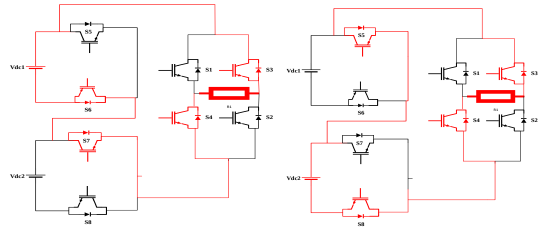
Three positive, three negative and one zero voltage level make the inverter output a 7-level RDC-MLI. The operating modes of the inverter circuit in all levels of the output voltage levels, as per respective time period i.e. 20 milli seconds from the respective 50 Hz frequency output

IV. OPERATING MODES.

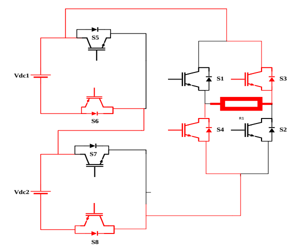


+V +2V

+3V 0V



-V -2V



-3V

Fig. 3. Operating modes (7-levels)

V. SIMULATION.

The simulation of this 7- level RDC-MLI is done on MATLAB-SIMULINK software. The simulation consists of two parts, the one inverter circuit, which comprises of 8 IGBts and two voltage sources. The other part of the simulation is the circuitry for the triggering of IGBTs. This circuitry comprises of combination of various logic gates, which are arranged in such a manner, such that the bridge part switches S1,S2,S3 and S4 are for polarity generation. S1, and S2 are triggered for positive half cycle of output voltage , whereas S3 and S4 contribute to the negative half cycle.

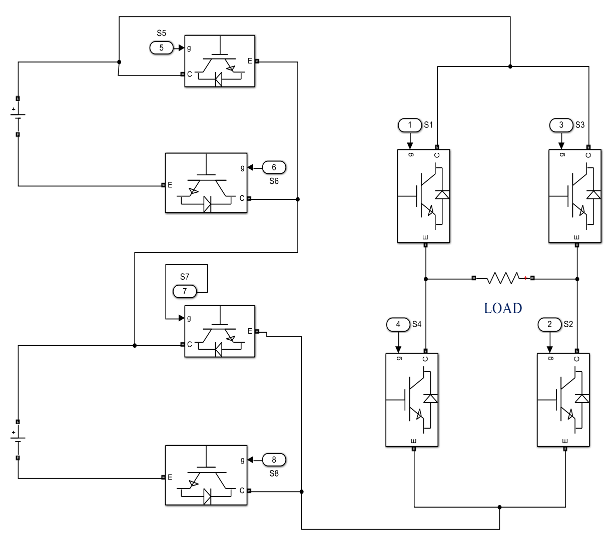


Fig. 4. Inverter circuit

To trigger these 8 IGBTs of this RDC-MLI logic gates are used, since we have to provide proper pulse to each IGBT at proper time so that respective required voltage level should be generated. In this regard the combination of XOR gates is employed for proper gate signal generation from the multicarrier triangular signals. Switches S1, S2, S3 and S4 are triggered with the help of zero carrier repeating carrier signal in such a way that the S1 and S2 are triggered.

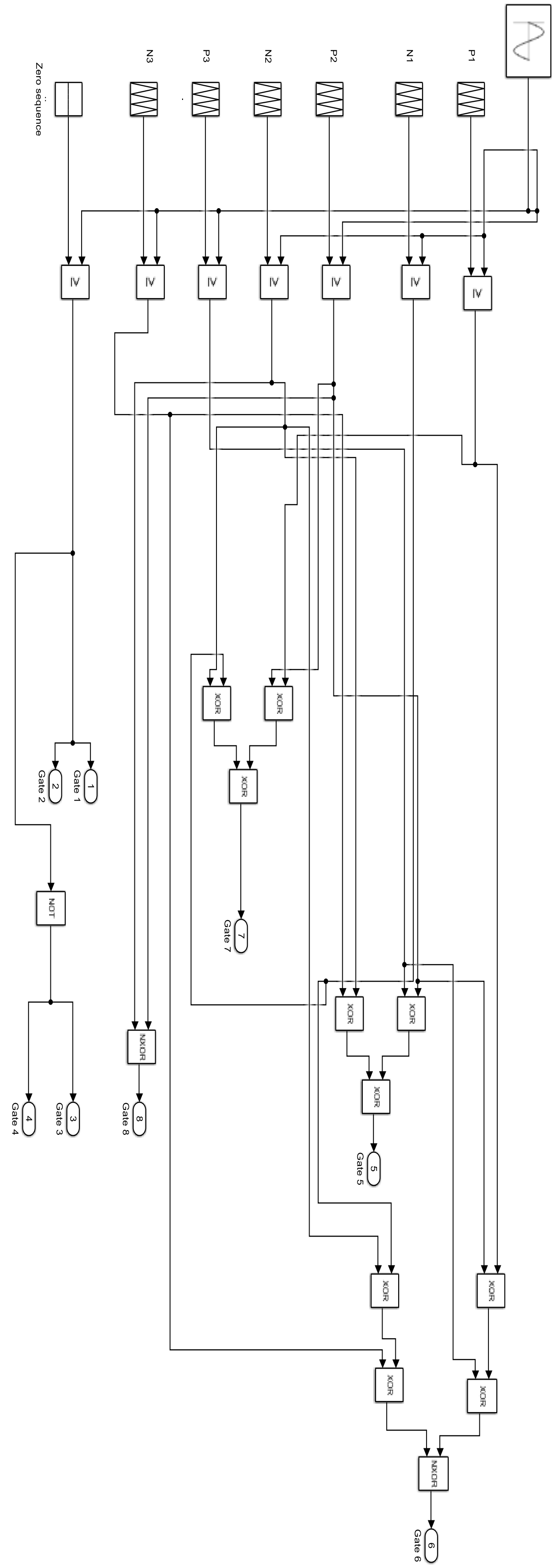


Fig. 5. Multicarrier PWM and pulses for gates.

VI. RESULT AND DISCUSION

The proposed RDC multilevel inverter, gives seven output levels by employing 8-IGBTs and two voltage sources. It should be noted that the proposed configuration is asymmetric in nature i.e. both the voltage sources have different voltage inputs.

The designed topology is superior to conventional CHB multilevel inverter in a sense that conventional CHB requires 8 IGBTs for 5- levels of output voltage and will require 12 IGBTs and three voltage sources in order to generate 7 level output. This relation of number of devices and output levels can be generalized for an N-level inverter by the (1)

$$No\ of\ switches = 4\left(\frac{N-1}{2}\right) \qquad \textbf{(1)}$$

And the number of input voltage sources in an N-level CHB multilevel inverter is given by the equation (2)

$$No\ of\ input\ dc\ sources = \frac{N-1}{2} \qquad (2)$$

Thus from the equations 1 and 2 it is clear that if 7- level output is to be generated with CHB- MLI the it will require 12 switches and three input dc sources. But the proposed topology uses only 8-IGBTs and 2 voltage sources. Thus the cost and complexity of the circuit has been reduced to a significant extent.

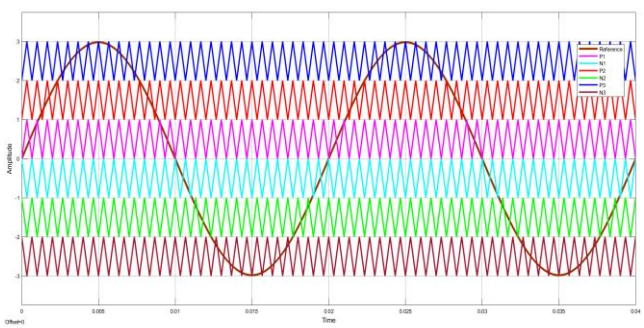


Fig. 6. High frequency carrier signals and reference sine wave.

The generated carrier signals are given to the relational operator, which are then given to logic gates, and in final the combination of logic gates are given to the gates of IGBTs. The output of the relational operator for three positive and three negative carrier signals is given.

Fig. 7. P1, P2 & P3 after comparator.

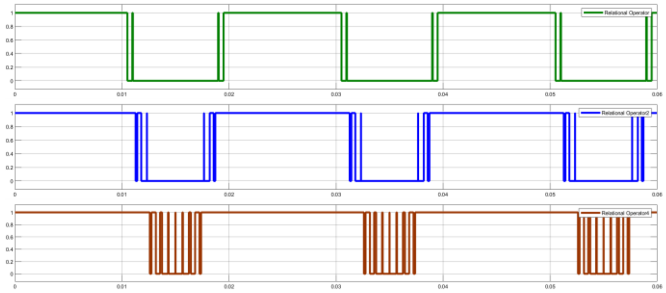


Fig. 8. N1, N2 & N3 after comparator.

The polarity generating switches are triggered in such a way that as per 50 Hz frequency, switches S1,S2 conduct for 10 milli seconds, whereas for negative half cycle S3,S4 contribute for the output voltage.

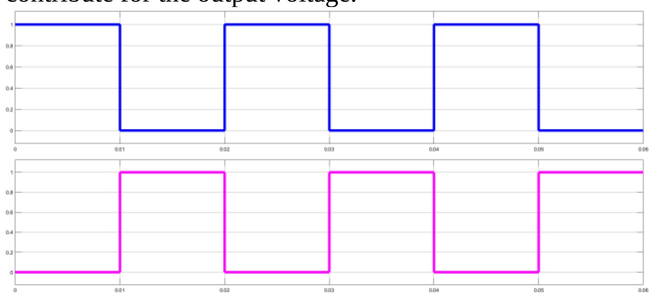


Fig. 9. Pulses for S1 and S2

The level generating switches triggered as per their respective voltage contribution.

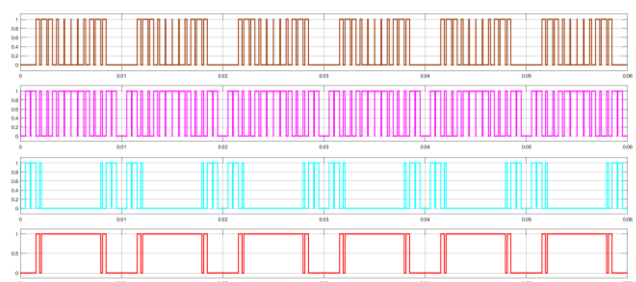


Fig. 10. Pulses for S5, S6, S7 and S8

The output voltage consists of 7 voltage levels. These 7 levels are obtained by total three positive, three negative and a zero level. The parameters of the simulation model are given in Table II

Table II Simulation Model Parameters

Model Parameters	
No. of Switches	8
No. of Dc Sources	2
Sine wave Frequency	1.5kHz
Resistive Load	100Ω
Output Voltage Levels	7
Carrier signals	6

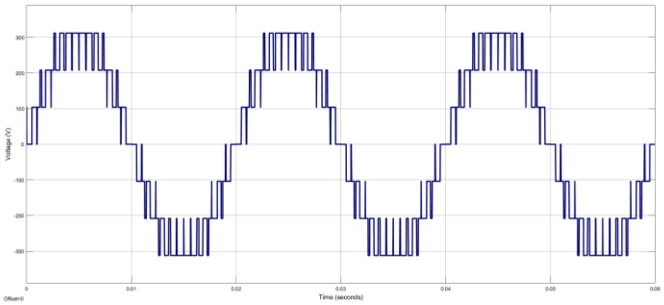


Fig. 11. Output Voltage waveform

Table III Input and Output voltages

Vdc1(V)	Vdc2(V)	$V_{out(}$rms) (V)
104	208	220

VII. HARMONICS ANALYSIS.

Power electronic converters have proved their worth in the field of electrical power systems, because of their high efficiency, but production of harmonics in power electronic converters is problem .Harmonics are nothing but multiples of fundamental frequencies.

The harmonics in any periodic waveform is determined by the following general Fourier series expression given in (3)

$$\boldsymbol{f(t) = a_o + \sum_{n=1,2,3......}^{\infty} (a_n Cos\ n\omega t + b_n Sin\ n\omega t)} \quad (3)$$

Where a_o is the DC component of the original wave, (a_n Cos $n\omega t$ + b_n Sin $n\omega t$) is the nth harmonic of the function. The values of a_o, a_n and b_n can be determined by the following relations.

$$a_o = \frac{1}{2\pi}\int_0^{2\pi} V_L(\omega t)\, d\omega t \quad (4)$$

$$a_n = \frac{1}{\pi}\int_0^{\pi} V_L(\omega t)\, Cos\ n\omega t\, d\omega t \quad (5)$$

$$b_n = \frac{1}{\pi}\int_0^{\pi} V_L(\omega t)\, Sin\ n\omega t\, d\omega t \quad (6)$$

Since all electrical machines are designed to operate at some particular frequency, if higher frequency components are passed, they cause serious power quality issues. Conventional single-phase H- bridge inverters, give output waveforms as square and quasi square waveforms. These waveforms contain certain harmonics, hence there are significant chances of power quality issues.

The more the waveform nearer to sine wave the lesser the harmonics it will contain and better will be the power quality. Therefore, multilevel inverters are making their roots in the field of power electronic converters. But as the number of levels are increased the number devices tend to increase proportionally. To resolve this issue the current trend in the research of power electronics is RDC-MLI.

The harmonic analysis was done using FFT tool of MATLAB-SIMULINK.

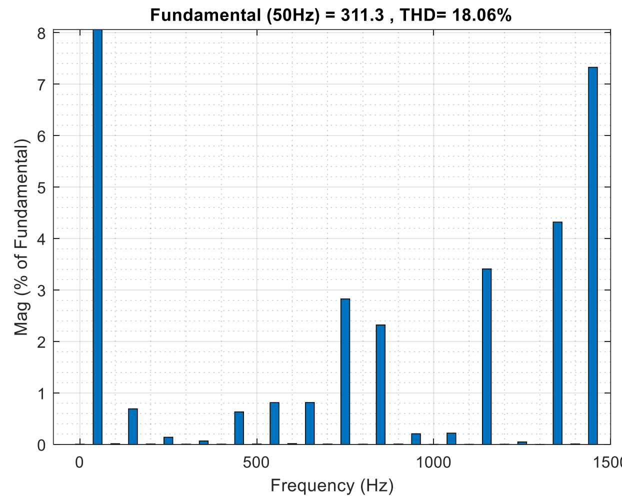


Fig. 12. THD Computation via FFT Tool.

VIII. CONCLUSION

A reduced device count multilevel inverter by using multicarrier PWM techniques, is designed. With the help of high frequency triangular carrier waves were simulated on MATLAB-SIMULINK. Increase in number of output voltage levels without increasing the complexity of circuits is the key feature of RDC-MLI. As the number of switching devices gets reduced, the switching losses also tend to reduce. The designed MLI provided 7 output voltage levels with 8 switches, if we try to get the same levels of output voltage by using conventional CHB-MLI it would have required 12 switches, and three voltage sources thus the complexity of the circuit would have increased, due to more switching devices and their gate drive circuits. PWM provide an effective way of triggering power electronic devices in current trends of power electronic converters. 1.5 kHz triangular carrier signal were generated which were one less than the obtained output voltage levels, thus if n- output levels are intended to be obtained n-1 carrier signals would be required. Multilevel inverters, producing stair case output waveform, by getting input from the conventional dc batteries or renewable sources is far better than the square and quasi-square waveform produced by the conventional H- bridge inverter. Moreover, the THD values in case of this RDC-MLI have been reduced significantly as compared to conventional H- bridge inverter well as MLIs.

REFERENCES

[1] Mahar, Mukhtiar Ahmed, Muhammad Aslam Uqaili, and Abdul Sattar Larik. "Harmonic analysis of ac-dc topologies and their impacts on power systems." *Mehran University Research Journal of Engineering & Technology* 30.1 (2011): 173-178.

[2] Govindaraju, C., and K. Baskaran. "Performance improvement of multiphase multilevel inverter using hybrid carrier based space vector modulation." *International Journal on Electrical Engineering and Informatics* 2.2 (2010): 137-149.

[3] Najafi, Ehsan, and Abdul Halim Mohamed Yatim. "Design and implementation of a new multilevel inverter topology." *IEEE transactions on industrial electronics* 59.11 (2011): 4148-4154.

[4] Tang, Qingquan, et al. "A new diode-clamping multilevel converter with reduced device count and DC voltage balancing control." *2009 IEEE Energy Conversion Congress and Exposition*. IEEE, 2009.

[5] Agrawal, Rekha, Jitendra Kumar Tandekar, and Shailendra Jain. "Multi-carrier pulse width modulation schemes for multilevel converters." *2016 IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS)*. IEEE, 2016.

[6] Karthik, A., and Umanand Loganathan. "A Reduced Component Count Five-Level Inverter Topology for High Reliability Electric Drives." *IEEE Transactions on Power Electronics* 35.1 (2019): 725-732.

[7] Su, Gui-Jia. "Multilevel DC-link inverter." *IEEE Transactions on Industry Applications* 41.3 (2005): 848-854.

[8] Prayag, Aparna, and Sanjay Bodkhe. "A comparative analysis of classical three phase multilevel (five level) inverter topologies." *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*. IEEE, 2016.

[9] Rani, P. Sudha, K. V. S. Prasadarao, and Koppineni RNV Subbarao. "Comparison of symmetrical and asymmetrical multilevel inverter topologies with reduced number of switches." *2014 International Conference on Smart Electric Grid (ISEG)*. IEEE, 2014.

[10] Bana, Prabhat Ranjan, et al. "Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: topologies, comprehensive analysis and comparative evaluation." *IEEE access* 7 (2019): 54888-54909.

[11] Gupta, Krishna Kumar, et al. "Multilevel inverter topologies with reduced device count: A review." *IEEE transactions on Power Electronics* 31.1 (2015): 135-151.

[12] Elahi, Md Fazla, and Md Aminul Islam. "A New Nine Level Inverter with Low TSV and Fewer Numbers of Components for Renewable Energy Systems." *2019 International Conference on Electrical, Computer and Communication Engineering (ECCE)*. IEEE, 2019.

[13] Bhatnagar, Pallavee, Rekha Agrawal, and Krishna Kumar Gupta. "Reduced device count version of single-stage switched-capacitor module for cascaded multilevel inverters." *IET Power Electronics* 12.5 (2019): 1079-1086.

[14] Aleenejad, Mohsen, et al. "Reduced number of auxiliary H-bridge power cells for post-fault operation of three phase cascaded H-bridge inverter." *IET Power Electronics* 12.11 (2019): 2923-2931.

[15] Agrawal, Nikhil, and Praveen Bansal. "A new 21-level asymmetrical multilevel inverter topology with different PWM techniques." *2017 Recent Developments in Control, Automation & Power Engineering (RDCAPE)*. IEEE, 2017.

[16] Bhargava, Vani, S. K. Sinha, and M. P. Dave. "A comparative modeling analysis of optimized multilevel inverter topologies with reduced device count for spv and wind integration." *2019 6th International Conference on Signal Processing and Integrated Networks (SPIN)*. IEEE, 2019.

[17] Siddique, Marif Daula, et al. "Low switching frequency based asymmetrical multilevel inverter topology with reduced switch count." *IEEE Access* 7 (2019): 86374-86383.

[18] Tang, Qingquan, et al. "A new diode-clamping multilevel converter with reduced device count and DC voltage balancing control." *2009 IEEE Energy Conversion Congress and Exposition*. IEEE, 2009.