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Comparative Performance Analysis of Conventional and Modular Multilevel Converter: A Research on Solar Based Application

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***Abstract*— Inverters are essential for converting DC input power into AC output power in power electronics systems. They are widely used to improve power quality and reduce harmonic content in sensitive loads. This research study focuses on evaluating different inverter configurations, including the Cascaded H-Bridge and neutral point clamped (NPC) inverters, as well as the modular multilevel converter (MMC), for a 5MVA PV array. Various pulse width modulation (PWM) control techniques such as alternate phase opposition deposition (APOD), in-phase deposition (IPD), phase opposite deposition (POD), and nearest level modulation (NLM) are employed to assess the performance of each inverter. The analysis is conducted using Matlab/Simulink software to determine the total harmonic distortion (THD) and provide insights into the harmonic content of the inverters.**

The comparative analysis reveals distinct trends in THD based on the control techniques employed. The Cascaded H-Bridge and NPC inverters, utilizing the POD PWM control technique, exhibit lower THD values compared to the IPD and APOD control schemes. In contrast, the MMC with NLM control demonstrates significantly lower THD than the Cascaded H-Bridge and NPC inverters using the POD control technique.

Furthermore, the research finds that increasing the number of levels in the inverter configuration leads to a decrease in THD, indicating improved harmonic mitigation and enhanced power quality. These findings provide valuable insights for selecting and optimizing inverter configurations, facilitating efficient and high-quality power conversion.

***Index Terms*— APOD, H–Bridge, IPD, MMC, NPC, NLM, POD, PWM, THD and MATLAB/ SIMULINK.**

I. INTRODUCTION

Renewable energy sources are increasingly replacing conventional energy sources, with solar PV arrays being widely adopted in residential, commercial, and industrial sectors. In these systems, inverters play a crucial role in converting the DC output of the PV array into AC power. However, the switching operations of modern multilevel inverters can introduce harmonic distortion, leading to various issues such as poor power factor, excessive heating, and transformer overloading. It is therefore important to use inverters with lower total harmonic distortion (THD) to meet harmonics standards like IEEE 519-2022.

Traditionally, low-voltage (LV) inverters convert DC voltage to AC, which is then stepped up to medium voltage (MV) using transformers or DC-DC converters before being connected to the AC grid. However, for MV applications, multilevel inverters are preferred over conventional two-level inverters due to their lower switching speed and better voltage blocking capabilities.

The Cascaded H-Bridge inverter uses multiple H-Bridge networks in a cascaded arrangement to generate multiple levels of output waveform. This arrangement eliminates the need for capacitors and diodes, resulting in reduced switching losses, filter size, and overall costs [1].

The Neutral Point Clamped (NPC) inverter is another MV inverter that ensures proper voltage sharing among all the switches using clamping diodes. NPC inverters are commonly used for medium voltage applications and offer advantages such as reduced switching losses, small output current ripple, and shared supply voltage. Increasing the voltage levels in NPC inverters can help further reduce THD and the size of required filters [2].

The Modular Multilevel Converter (MMC) was initially designed for high-voltage direct current (HVDC) applications but has shown potential for MV applications as well. MMC provides modularity, low switching losses, and eliminates the need for additional filters by utilizing the fundamental frequency. It is capable of achieving high efficiency and low THD, making it suitable for medium and high voltage applications [3].

This research paper aims to address the research gap in the application of MMC converters for MV systems. The paper provides a comprehensive overview of PV solar panels, MMC converters, H-Bridge converters, and NPC converters. Each converter is described in detail, including circuit diagrams, control techniques, and operational waveforms for various levels. The THD of each converter is then compared to evaluate their performance.

In summary, this paper presents an in-depth analysis of different inverters used in PV systems, including their configurations, control techniques, and THD characteristics. The findings will contribute to the selection and optimization of inverters for medium voltage applications, ensuring efficient and high-quality power conversion.

II. PV SOLAR PANEL

Photovoltaic (PV) panels are utilized to generate DC input voltages, which are then fed into inverters. These PV panels harness sunlight as their source, making them particularly effective during daylight hours. PV model data, such as open circuit voltage, short circuit current, and maximum power points, are provided under standard test conditions, involving an irradiance of 1000 W/m^2 and a temperature of 25°C. The output of the PV panel can be boosted to meet the required voltage specifications. This process involves the conversion of solar radiation into electricity through the photovoltaic effect, forming the foundation of solar-based electricity generation [4]. Figure 1 depicts a block diagram illustrating the generation of electric power through a PV panel.

Fig 1: Block diagram.

III. MODULAR MULTILEVEL CONVERTER

The modular multilevel converter (MMC) consists of upper and lower arms, each composed of a series connection of sub-modules. These sub-modules are comprised of half bridges, which consist of two switches and one parallel-connected diode. The diodes play a crucial role in controlling the flow of current. Additionally, an inductor is connected to both arms to limit the fault current and minimize the potential difference between the two arms [5].

The presence or absence of a capacitor in each sub-module depends on the current state of the capacitor. There are three functioning states: cut-in state, cut-off state, and blocking state. In the cut-in state, the capacitor is inserted, and only sub-module 1 (SM1) is ON. In the cut-off state, the capacitor is not inserted, and sub-module 2 (SM2) is ON. In the blocking state, both sub-modules are OFF, and only one diode is ON. Specifically, the capacitor is inserted when D1 is ON, and it is not inserted when D2 is ON, as illustrated in Table 1.

TABLE 1: Operation of Sub module

State	SMO$_1$	SMO$_2$	D1	D2	State of Capacitor
Cut In State	ON	OFF	-	-	Inserted
Cut OFF State	OFF	ON	-	-	Not Inserted
Blocking State	OFF	OFF	OFF & ON	ON & OFF	Not Inserted Inserted

The output voltage equations for upper arm eq. (1) and lower arm eq. (2):

$$V = \frac{VDC}{2} - V1 - V2 \qquad (1)$$

$$V = -\frac{VDC}{2} + V3 + V4 \qquad (2)$$

Where (V) is voltage output of arm whereas V_{DC} is the input dc voltage and ($V_{1\text{-}4}$) are the sub module voltages. Desired voltage level is attained when different upper and lower arm sub modules are connected and disconnected. Modular multilevel inverter circuit diagram is shown below in Fig 2.

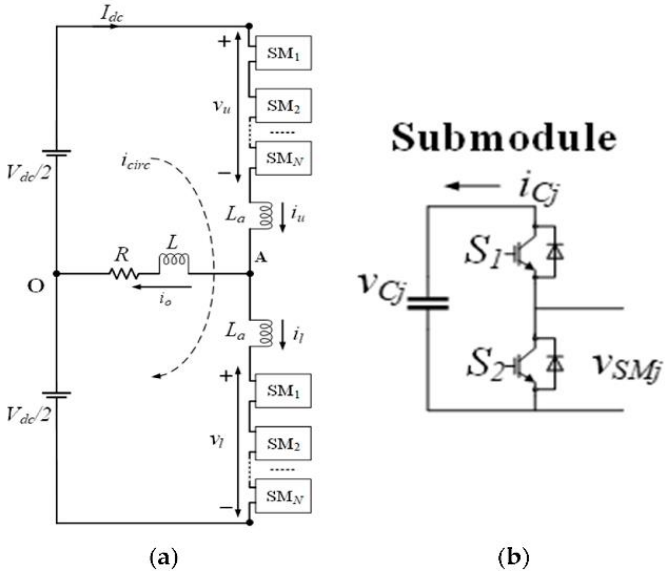

Fig 2: (a). Basic circuit diagram for MMC.
(b). Sub module for MMC

The control technique, which is used to implement MMC, is nearest level modulation (NLM) that is alternative to carrier based modulation control technique. This control technique is simple and easy to implement previously used for the large drive multi-level systems, because it is easy digitally implement during operation at high levels and flexible to use for MMC [5]. Main advantage of this technique is that it is free from many carrier waveforms and computed by its switching states and Duty cycles. In this a Reference wave mostly Sinusoidal waveform is used at (fundamental frequency) and approximated it to the next level of Integer i.e. we have 0.6 so it is approximated to 1. So reference waveform gets staircase shape so now for N levels of MMC, there will be N+1 levels of NLM. If frequency of inverter is higher than approximation will be better and better [5]. The Fig 3 and 4 shows block diagram and working principle for NLM.

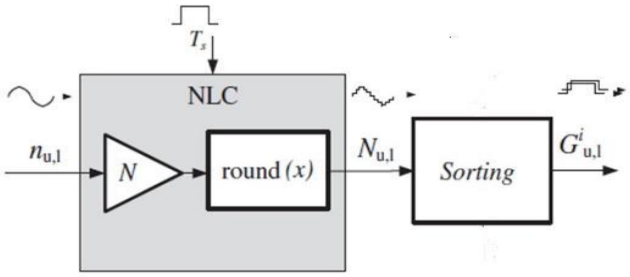

Fig 3: NLM block diagram.

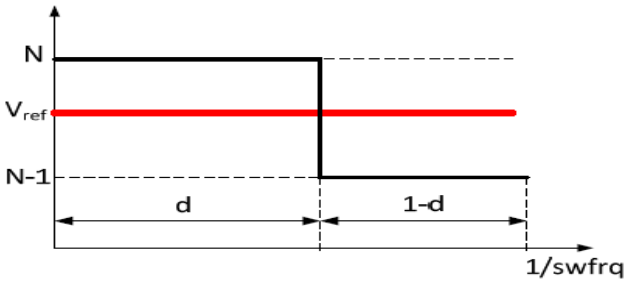

Fig 4: NLM Working Principle.

IV. CASCADED H-BRIDGE CONVERTER

The main advantage of Cascaded H Bridge Inverter is that it does not require a diode Capacitor. It is Multi level Inverter and made up of series Connected H Bridges that are energized by separate DC Supply [6] For 5 Level inverter output voltage vary from +2 V_{DC} to -2 V_{DC} and we create 5 in-between levels. These voltage levels are attained by using different switches. One full series of H Bridges make one phase of the Inverter, which generates several output voltage levels, also it provides phase balance of AC system [7]. This Arrangement of H Bridge is used for the application of high power and high Voltage applications as this arrangement decreases load on the switch in comparison to unipolar and bipolar inverters [8] Other advantage is that voltage and power can be increased in safer limits and noise interferences can be reduced. The circuit diagram for 5 level cascaded H Bridge Inverter is shown in Fig 5 that consists of 2 series connected H Bridges, 2 dc voltage sources. The output voltage is the sum of both H bridges [9].

$$V = V1 + V2 \qquad (3)$$

Where (V) is the output voltage and V_1 is the first H-bridge voltage and V_2 voltage across second H-bridge.

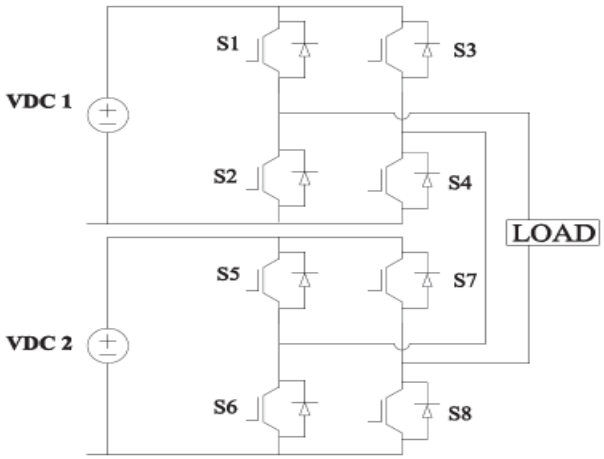

Fig 5: Circuit diagram for 5 level cascaded h bridge inverter.

We use sinusoidal pulse width modulation (SPWM) control method is used to power this inverter and its three types are in phase deposition (IPD), the phase opposition deposition (POD) and alternate phase opposition deposition (APOD) [10].

A. In Phase Deposition (IPD)

In the IPD all triangular carriers are in phase to one another as shown in Fig 6.

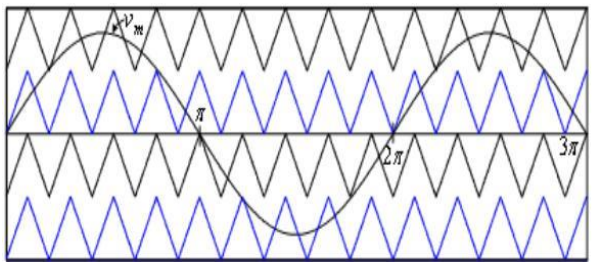

Fig 6: IPD control scheme.

B. Phase- opposition deposition (POD)

In POD above reference line all carriers are in phase to each other and below the reference line all carriers are 180^0 out of phase as shown in Fig 7.

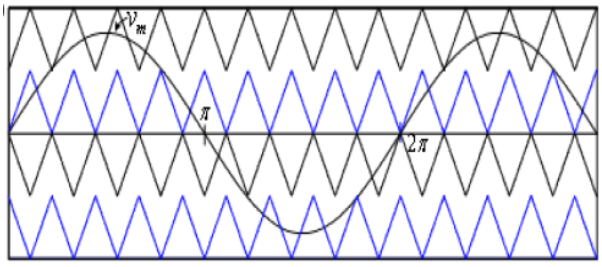

Fig 7: POD control scheme.

C. Alternate phase opposition deposition (APOD)

In APOD one carrier is in phase and the other is out of phase by 180^0 from the first one alternatively as shown in the Fig 8.

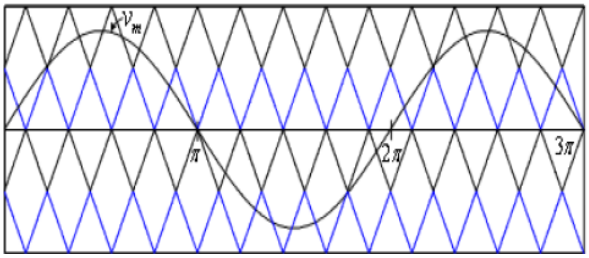

Fig 8: APOD control scheme.

V. NEUTRAL POINT CLAMPED (NPC) INVERTER

NPC inverters, also known as diode clamped inverters, are a type of multilevel power inverter. They utilize clamping diodes to ensure proper voltage sharing among power switches, resulting in improved performance with reduced complexity. NPC inverters offer superior waveform quality and have the advantage of minimizing the need for additional filters [11]. They are commonly used in medium voltage applications.

In a 3-level NPC inverter, each leg consists of four switches. For an M-level inverter, the configuration includes 2 x (M-1) dc links and (M-1) x (M-2) clamping devices, providing increased voltage levels and flexibility [12]. Figure 9 illustrates a 3-level NPC inverter, where the DC voltages are split between two capacitors, C1 and C2, resulting in a midpoint neutral point (N). The output voltage of a 3-level NPC inverter can have three states: VDC/2, 0, and -VDC/2 [13]. The switch status required to achieve the desired output levels is presented in Table 2, and Figure 10 depicts the pulse width modulation (PWM) control for a 3-level NPC inverter [9].

TABLE 2: Switching Pattern for 3-Level NPC

ON Switches	OFF Switches	Voltage Output (Vo)
S_1, S_2	S_3, S_4	$+V_{DC}/2$
S_2, S_3	S_1, S_4	0
S_3, S_4	S_1, S_2	$-V_{DC}/2$

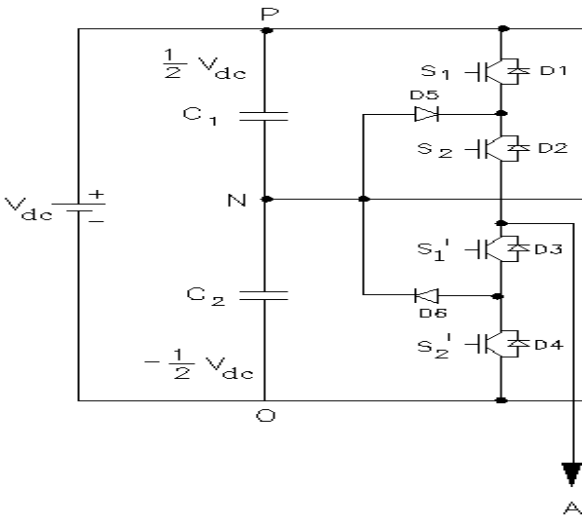

Fig 9: 3- level NPC inverter circuit diagram.

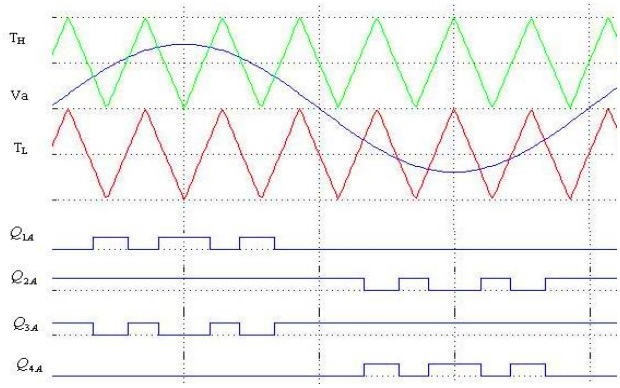

Fig 10: 3 Level NPC inverter (PWM) control.

In this technique, a reference sinusoidal waveform is compared with two triangular carrier waveforms to generate pulses. The pulses ($Q_{1\text{-}4A}$) are generated when we compare (Va) with (T_H) and (T_L) respectively. The switch Q_{1A} is on when $Va>T_H$, Q_{4A} is on when $Va>T_L$, Q_{3A} is on when Q_{1A} off, Q_{2A} is on when Q_{4A} off [14].

VI. COMPARATIVE ANALYSIS OF MODULAR MULTILEVEL INVERTER, H-BRIDGE AND NEUTRAL POINT CLAMPED INVERTER

Comparative analysis done by using MATLAB/Simulink software. Comparison is done in terms of total harmonics distortions THD for the 3, 5,7 and 9 levels.

A. For 3 Levels

1) MMC 3-Level

MMC 3 level Voltage waveform and THD are shown in Figures 11 and 12.

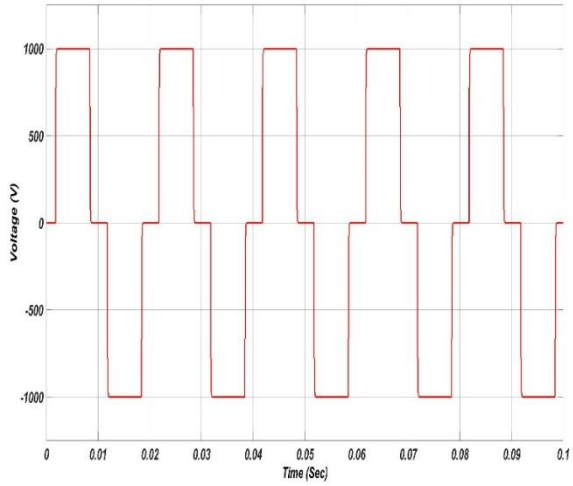

Fig 11: 3 level MMC output voltage waveform.

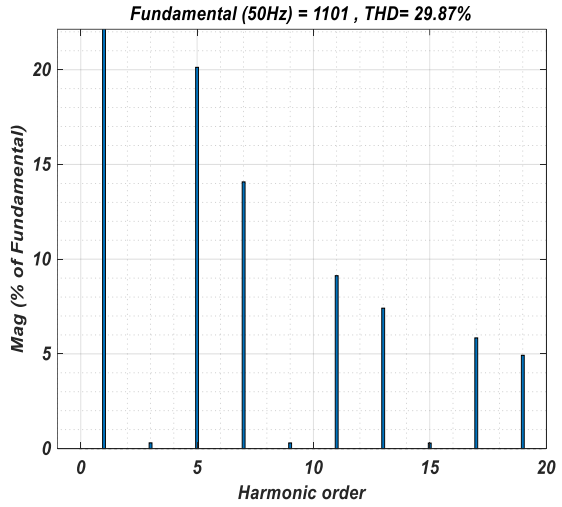

Fig 12: 3-Level MMC THD Analysis.

For 3-level MMC by using NLM control technique we have Resistive load of 100 ohms for that there is THD of 29.87%.

2) Cascaded H-Bridge 3-Level Inverter

A 3 level Voltage waveform and THD by using POD technique for cascaded H Bridge Inverter are shown in Figures 13 and 14 and THD comparison for IPD, POD and APOD in Table 3.

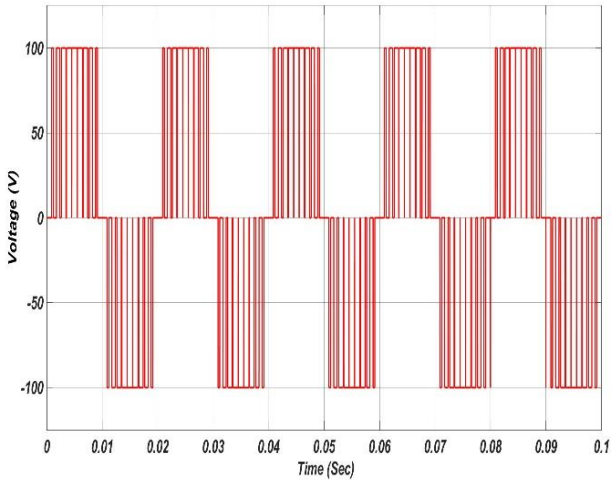

Fig 13: Output voltage for 3-Level H-Bridge.

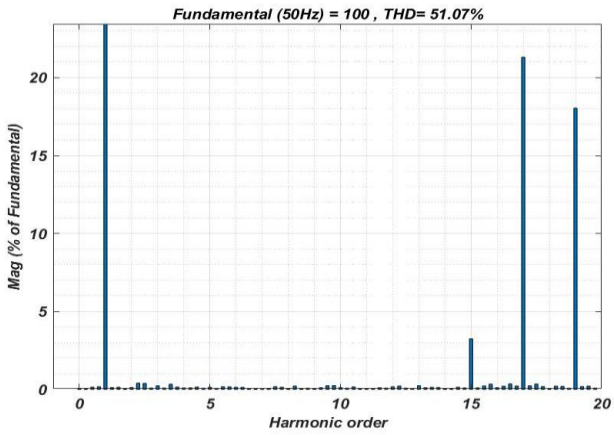

Fig 14: THD for 3-level H-bridge using POD**.**

TABLE 3: 3-Level H Bridge THD Analysis

Name of Scheme	THD in %
APOD	51.09%
IPD	51.85%
POD	51.07%

For 3-level H-Bridge by using POD control technique when resistive load of 100 ohms for that there is THD of 51.07% which is better than IPD and APOD control technique.

3) NPC 3-level

For 3-Level NPC output voltage and THD for POD control technique shown in Figure 15 and 16 and THD using IPD, POD, APOD schemes in Table 4.

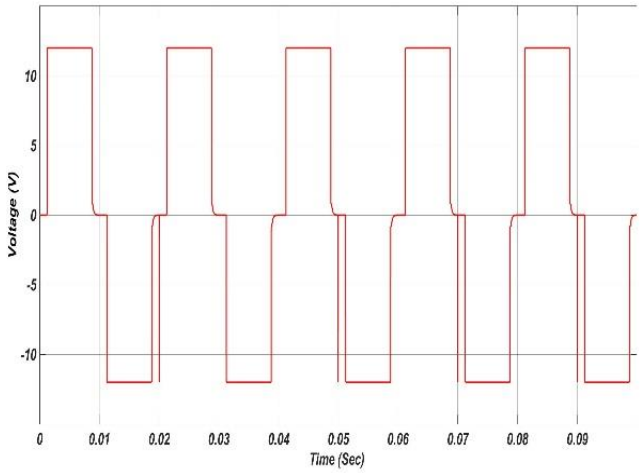

Fig 15: Output voltage for 3-level NPC using POD.

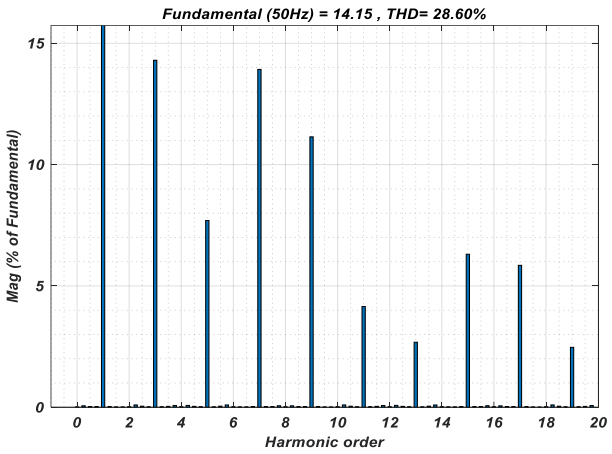

Fig 16: THD for 3 level NPC using POD.

TABLE 4: 3 Level NPC THD Analysis

Name of Scheme	THD in %
APOD	28.60%
IPD	31.45%
POD	28.60%

For 3-level NPC by using POD control technique when Resistive load of 100 ohms for that there is THD of 28.60% which is better than IPD and APOD control technique.

B. For 5- Levels

1) 5-Level MMC

MMC 5 level Voltage waveform and THD are shown in figures 17 and 18.

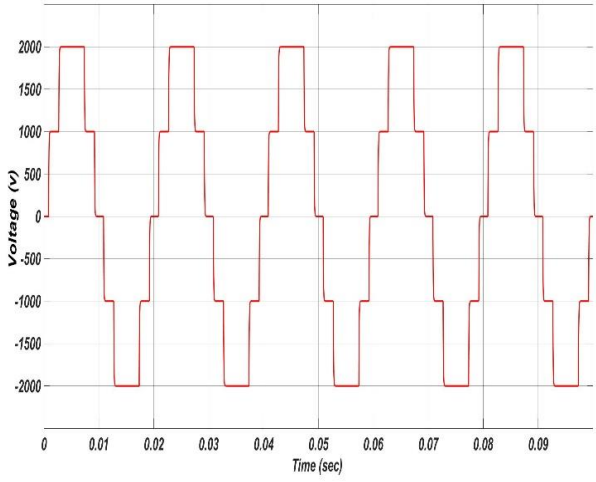

Fig 17: 5 level MMC Output Voltage Waveform.

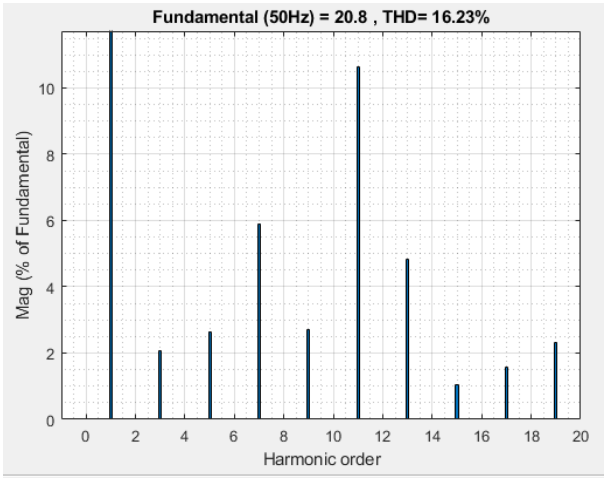

Fig 18: 5-Level MMC THD Analysis.

For 5-level MMC by using NLM control technique when there is Resistive load of 100 ohms for that there is THD of 16.23%.

2) Cascaded H-Bridge 5-Level Inverter

5 level Voltage waveform and THD by using POD technique for cascaded H Bridge Inverter are shown in figures 19 and 20 and THD for IPD, POD and APOD in Table 5.

TABLE 5: THD Analysis for 5-Level H Bridge

Name of Scheme	THD in %
APOD	27.98%
IPD	30.73%
POD	26.12%

For 5-level H-Bridge by using POD control technique when Resistive load of 100 ohms for that there is THD of 26.12% which is better than IPD and APOD control technique.

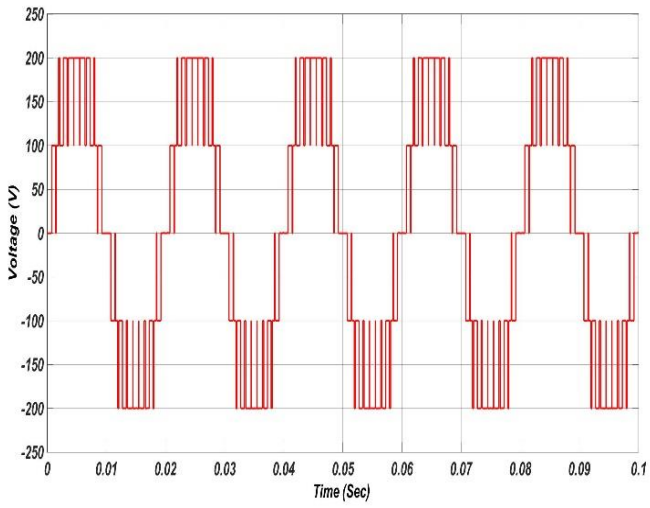

Fig 19: 5- Level H-Bridge Output Voltage Using POD control Scheme.

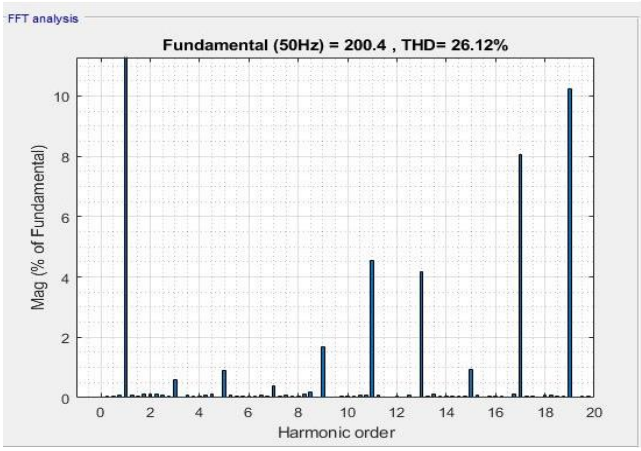

Fig 20: THD for 5-level H-Bridge using POD.

3) NPC 5-level

For 5-Level NPC output voltage and THD for POD control technique shown in Figure 21 and 22 and THD using IPD, POD, APOD schemes in Table 6.

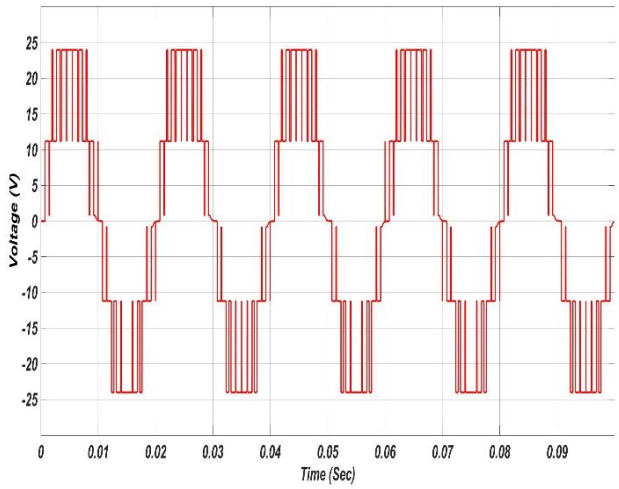

Fig 21: Output Voltage for 5-level NPC using POD.

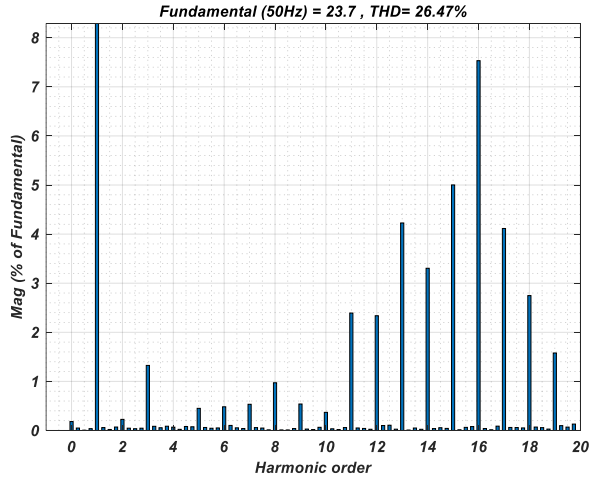

Fig 22: THD for 5 level NPC using POD.

TABLE 6: THD Analysis for 5 Level NPC

Name of Scheme	THD in %
APOD	28.35%
IPD	27.25%
POD	26.47%

For 5-level NPC by using POD control technique when Resistive load of 100 ohms for that there is THD of 26.47% which is better than IPD and APOD control technique.

C. For 7- Levels

1) 7-Level MMC

MMC 7 level Voltage waveform and THD are shown in Figures 23 and 24.

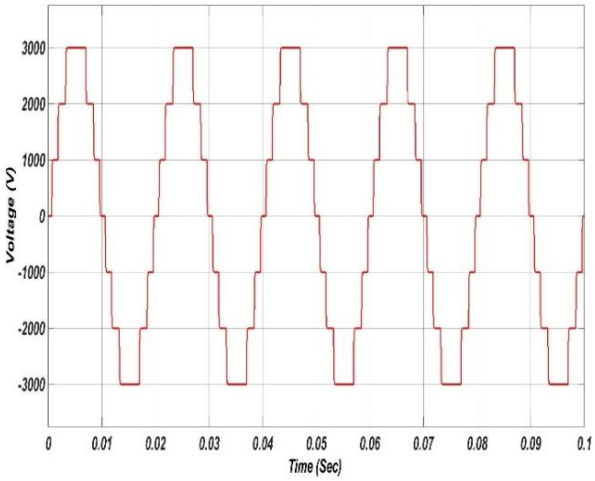

Fig 23: 7 level MMC Output Voltage Waveform.

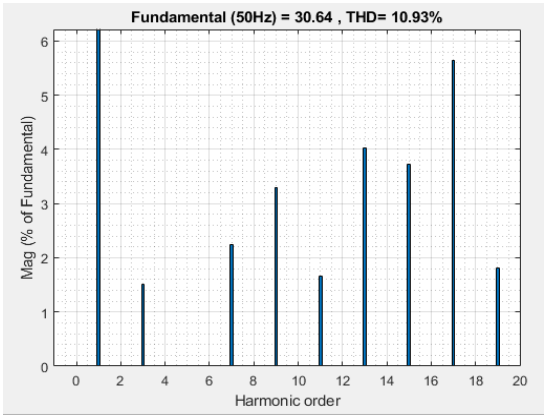

Fig 24: 7-Level MMC THD analysis.

For 7-level MMC by using NLM control technique we have Resistive load of 100 ohms for that there is THD of 10.93%.

2) Cascaded H-Bridge 7-Level Inverter

7 level Voltage waveform and THD by using POD technique for cascaded H Bridge Inverter are shown in Figures 25 and 26 and THD for IPD, POD and APOD in Table 7.

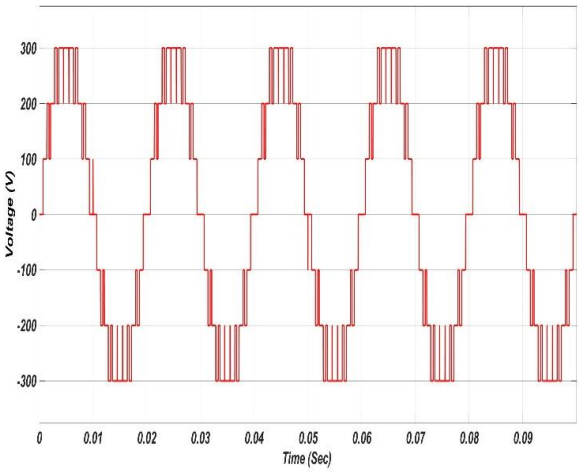

Fig 25: Output Voltage for 7-Level H-Bridge using POD Control Scheme.

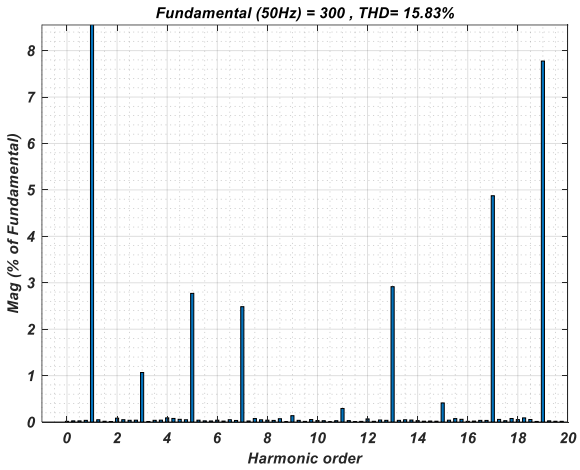

Fig 26: THD for 7-level H-Bridge using POD.

TABLE 7: THD Analysis For 7 Level H-Bridge

Name of Scheme	THD in %
APOD	18.39%
IPD	17.76%
POD	15.83%

For 7-level H-Bridge by using POD control technique when Resistive load of 100 ohms for that there is THD of 15.83% which is better than IPD and APOD control technique

3) NPC 7-level

For 7-Level NPC output voltage and THD for POD control technique shown in Figure 27 and 28 and THD using IPD, POD, APOD schemes in Table 8.

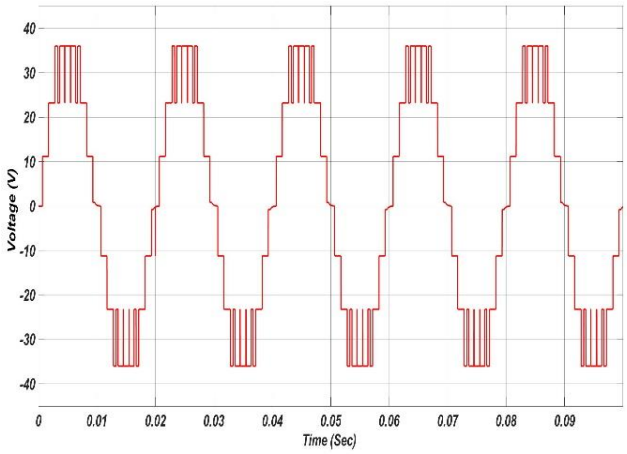

Fig 27: Output Voltage for 7-level NPC using POD.

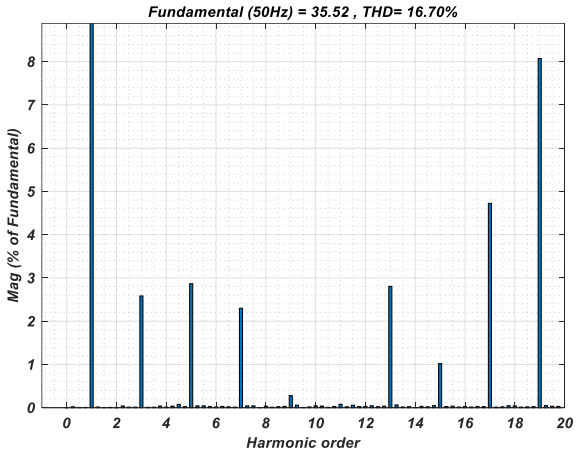

Fig 28: THD for 7 level NPC using POD.

TABLE 8: THD Analysis For 7 Level NPC

Name of Scheme	THD in %
APOD	19.89%
IPD	18.39%
POD	16.70%

For 7-level NPC by using POD control technique when Resistive load of 100 ohms for that there is THD of 16.80% which is better than IPD and APOD control technique

D. For 9- Levels

1) 9-Level MMC

The MMC 9 level voltage waveform and THD are shown in Figures 29 and 30.

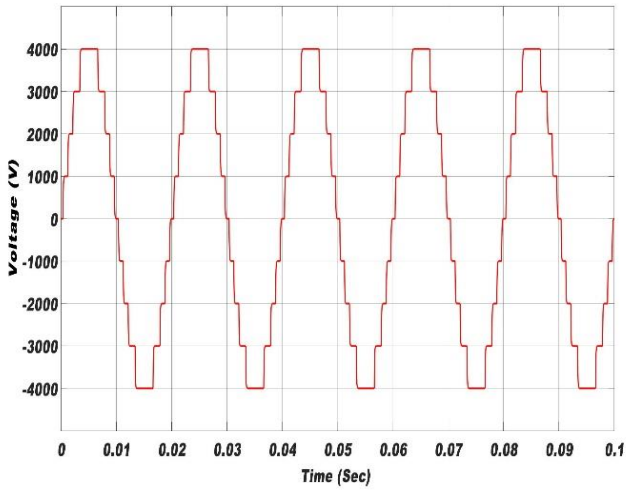

Fig 29: 9-level MMC Output Voltage Waveform.

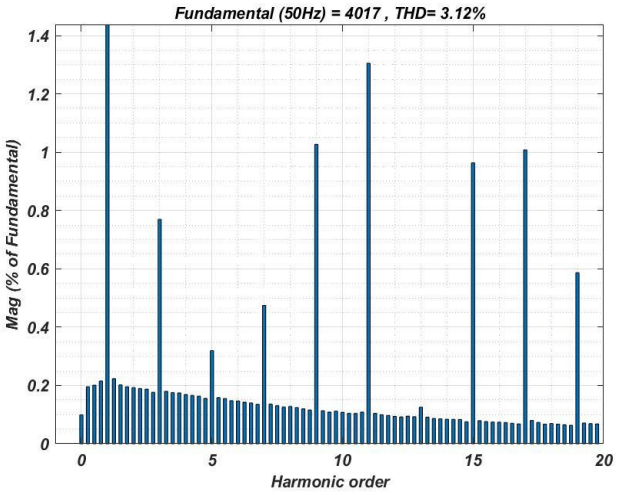

Fig 30: 9-Level MMC THD.

For 9-level MMC by using NLM control technique we have Resistive load of 100 ohms for that there is THD of 3.12%.

2) Cascaded H-Bridge 9-Level Inverter

9 level Voltage waveform and THD by using POD technique for cascaded H Bridge Inverter are shown in figures 31 and 32 and THD for IPD, POD and APOD in Table 9.

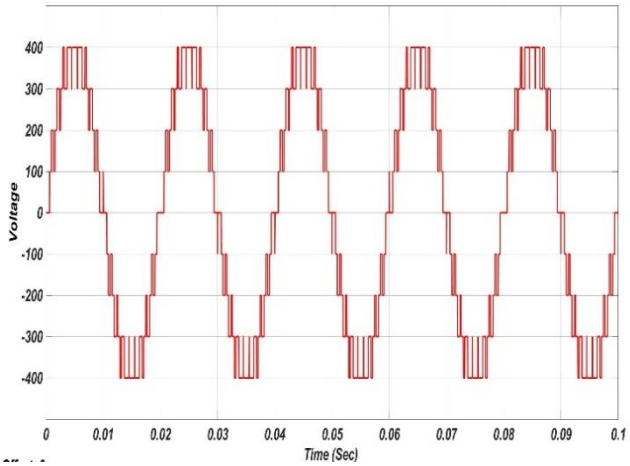

Fig 31: Output voltage for 9-Level H-Bridge using POD control scheme.

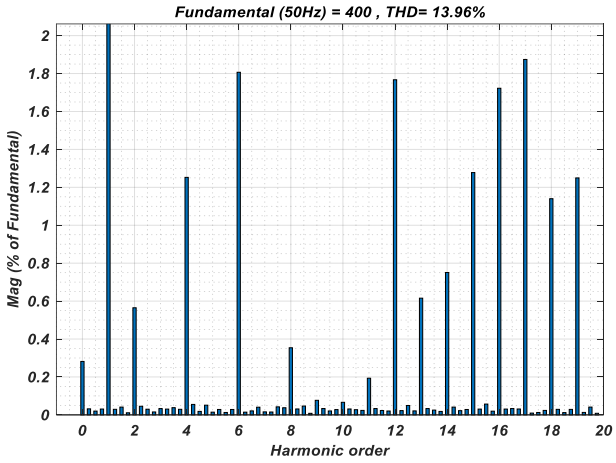

Fig 32: THD for 9-level H-Bridge using POD.

TABLE 9: THD Analysis For 9 Level H-Bridge

Name of Scheme	THD in %
APOD	14.28%
IPD	15.22%
POD	13.96%

For 9-level H-Bridge by using POD control technique when Resistive load of 100 ohms for that there is THD of 13.96% which is better than IPD and APOD control technique.

3) NPC 9-level

For 9-Level NPC output voltage and THD for POD control technique shown in Figure 33 and 34 and THD using IPD, POD, APOD schemes in Table 10.

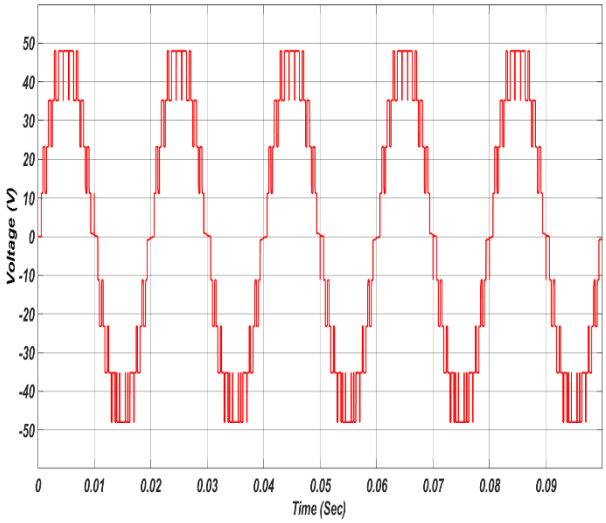

Fig 33: Output Voltage for 9-level NPC using POD.

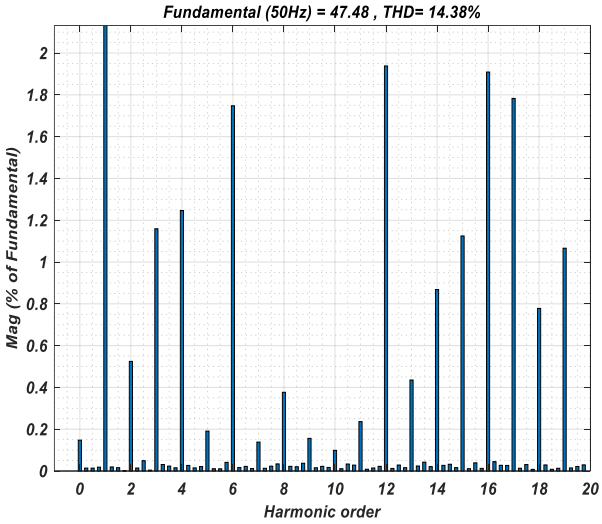

Fig 34: THD for 9 level NPC using POD.

TABLE 10: THD Analysis for 9 Level NPC

Name of Scheme	THD in %
APOD	14.72%
IPD	15.65%
POD	14.38%

For 9-level NPC by using POD control technique when Resistive load of 100 ohms for that there is THD of 14.36% which is better than IPD and APOD control technique

VII. RESULTS

A. *THD Analysis*

Based on the comparative analysis of the MMC, NPC, and Cascaded H-Bridge inverters, the findings indicate distinct trends in terms of total harmonic distortion (THD) based on the control techniques employed. The POD PWM control technique utilized in the Cascaded H-Bridge and NPC inverters demonstrates lower THD values compared to the IPD and APOD control schemes. On the other hand, the MMC, with its NLM control technique, exhibits significantly lower THD than both the Cascaded H-Bridge and NPC inverters using the POD control technique.

Furthermore, the results highlight that increasing the number of levels in the inverter configuration leads to a decrease in THD. This indicates that the inclusion of additional levels enhances the ability of the inverter to mitigate harmonic distortions, resulting in improved power quality.

The Summarized results of Comparative Analysis in terms of THD is shown in Table 11.

TABLE: 11 Summarized Comparison of THD Analysis For Converters.

S:NO	Level	MMC	Cascaded H-Bridge (POD)	NPC (POD)
1	3	29.87%	51.09%	28.60%
2	5	16.21%	26.12%	26.85%
3	7	10.93%	15.89%	16.69%
4	9	3.12%	13.96%	14.38%

VIII. CONCLUSIONS

The analysis of total harmonic distortion (THD) for all the inverters reveals important insights. The cascaded H-Bridge inverter utilizing the POD scheme demonstrates superior performance compared to the NPC inverter, particularly in the context of the 3-level configuration. On the other hand, the MMC exhibits even lower THD values than both the H-Bridge and NPC inverters.

Furthermore, the results indicate a clear trend: as the number of levels in the MMC increases, the THD decreases progressively. Similarly, the THD of the NPC and cascaded H-Bridge inverters also decreases with increasing levels, albeit to a lesser extent compared to the MMC.

The THD analysis also highlights an important relationship between the number of output voltage levels and waveform quality. Increasing the number of levels leads to a reduction in THD and brings the output voltage waveform closer to a sinusoidal shape. This improvement in waveform quality allows for a reduced filter size requirement. Notably, the MMC demonstrates significantly lower THD values, eliminating the need for an additional filter.

In particular, the 9-level MMC configuration achieved a THD of 3.12%, which complies with the IEEE standards 519-2022. This value is three times lower than the THD obtained from the H-Bridge and NPC inverters. These results solidify the recommendation to utilize the MMC for medium voltage applications and power supply to the grid, as it ensures minimal distortions in the electrical system.

By employing the MMC, power can be delivered to the grid with improved power quality and reduced harmonic

distortions. This technology offers a promising solution for enhancing the performance and efficiency of medium voltage applications, while meeting the stringent requirements set by industry standards.

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