International Journal of Electrical Engineering & Emerging Technology, Vol. 06, No. 01, JUN 2023, pp 8-12

Performance Assessment of Hybrid Multilevel Inverter with Bipolar Multicarrier Technique

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[**Received on:** 14/05/2023 **Accepted on**: 01/06/2023 **Published on:** 21/06/2023]

***Abstract*— Inverters have gained much popularity in last few decades. With regard to efficiency and less complicated circuits, there are numerous inverter topologies. This paper primarily focuses on reducing the number of devices in an inverter using the proposed topology. This study presents performance analysis of hybrid MLI using phase disposition bipolar multicarrier technique with improved efficiency in MATLAB/SIMULINK. The major concern of this project is to evaluate the performance of hybrid MLI topology having reduced number of semiconductor switches and comparatively high efficiency from the conventional topologies.**

***Index Terms*— Hybrid MLI, Phase Disposition, total harmonic distortion, pulse width modulation (PWM).**

I. INTRODUCTION

CONVERTER that generates AC power from DC power is known as an inverter. The output retrieved from these inverters often produce constant frequency and Voltage. Inverters have many useful applications in different power electronic circumstances. It is highly used for the inversion of battery power to sinusoidal Alternating Current (AC) and the same AC voltage is stepped up and sent in the form of rectified (HVDC) transmission over a long distance In practical it produces non-sinusoidal output because of harmonic distortion. Harmonics in output are reduced with increase in voltage levels at output, with help of switching of power switches along with other switching techniques. Multilevel inverters are the most often used in power electronics because they have lower harmonic distortion and radio frequency interference. Colak, Kabalci, and Bayindir [3]. The power electronic studies explicitly state that increasing number of levels improves the performance of multilevel waveforms. Different topologies have been created in multilevel inverters to lower the number of devices without sacrificing performance. It is possible to control an inverter's output with fewer distortion losses by using the proper pulse width modulation algorithms. Two categories of symmetric and asymmetric DC sources make up the input DC sources. J. Dixon and J. Pereda [9]. When symmetric sources are taken into account, all DC sources have the same magnitude. In contrast, the input DC sources of the level generating mode and the auxiliary module are of different magnitudes in the asymmetric category.

Over the past few decades, multilevel inverters (MLIs) have become incredibly popular. To lower overall harmonic distortion and boost power quality and output waveform, researchers are attempting to explore for an increasing number of levels. Although the less distorted waveform is quite close to a perfect sinusoidal wave, there will always be some distinguishing features. The number of components and switching losses rise as the number of voltage levels and switching devices increases.

This paper is structured as follows. Section II deals with the MATLAB simulation of hybrid nine level multilevel inverter along with working principle. In section III, bipolar multicarrier pulse width modulation technique is explained which is used in this paper. Output voltage and its total harmonic distortion is discussed in section IV. In section V, conclusion is discussed.

II. PROPOSED HYBRID MULTILEVEL INVERTER

The proposed hybrid MLI uses less switches to provide a greater number of levels. It enables the several dc voltage sources to run in parallel. MATLAB /SIMULINK model of proposed hybrid multilevel inverter is mentioned in Fig. 1.

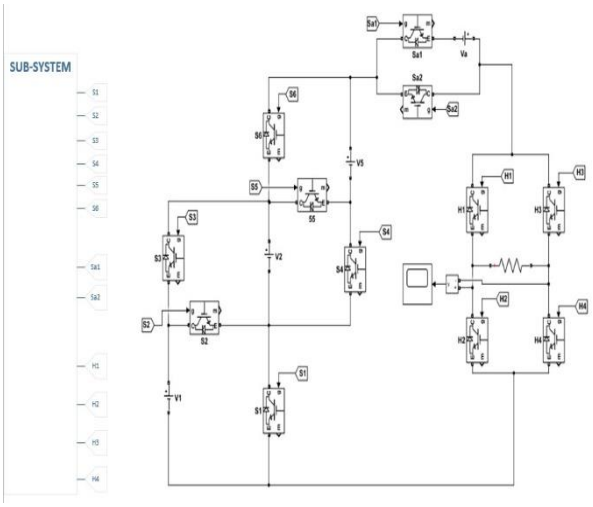

Fig: 1 MATLAB/SIMULINK Model of proposed hybrid multilevel inverter.

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Simply integrating two or more different topologies results in hybrid MLI. Compared to typical multilevel inverters, it has fewer components and carrier signals. It also offers less switching disturbances than traditional MLIs. As a result, there is less voltage stress across the IGBTs. The hybrid MLI topology may generate more output voltage levels while utilizing less power switches and dc voltage sources. It is made up of three components: a polarity-changing unit, an auxiliary module, and a level generation module. Positive polarity voltage is produced by the level generation module. After the LGM, an auxiliary module is attached to create more levels at the output. Positive and negative voltage levels can be achieved at the output by using a polarity changing unit.

Working Principle

The model has four DC input sources (Vdc and Va), each of which provides 30 volts of voltage. The magnitude of the DC voltage sources linked in the level generator module and auxiliary module determines the output levels. I focused on symmetrical setup, where Vdc = Va in this mode. As a result, N=(K+2)+1, where K is total number of levels, is presented as the number of output levels. This architecture uses 12 switches for the two cells, as determined by Ns = 3 (k + 2). For the proposed hybrid MLI to work in parallel, the size of the DC sources connected to the LGM must be equal. The operating modes are chosen in accordance with the IGBT switching frequencies, which regulate the operating circumstances of the active devices. The load receives nine levels of output voltage: Vdc, 2Vdc, 3Vdc, 4Vdc, and zero for E1=E2=Vdc. For every positive output voltage levels at the output, switches H1 and H4 are always in conducting state, while H2 and H4 are in blocking states. For every negative output voltage levels switches H2 and H4 are in ON condition. However, H1 and H3 must be in OFF states. Only H2 and H4 conduct currents in mode 1, while all other switches are in the off position. Hence there is no current will flow through the load because power switch work in complementary pairs. . In mode-2, S1/S3, S4/S6, Sa2, H1 and H4 conduct and remaining all switches in off state, Vdc will appear at the output. In mode-3, S2, S4/S6, Sa2, H1 and H4 conduct the current and remaining switches are in off state, while 2Vdc will appear across the load. For mode-4, S2, S5, Sa2, H1 and H4 conduct the current and remaining switches are in off state, due to these switches 3Vdc will appear across the load. In mode-5, S2, S5, Sa1, H1 and H4 switches conduct and remaining switches are in blocking condition while $4V_{dc}$ will appear at the load. Moreover, in other modes current flow through different switches and voltages appear at the output in reverse direction.

III. BIPOLAR MODULATION CONTROL SCHEME

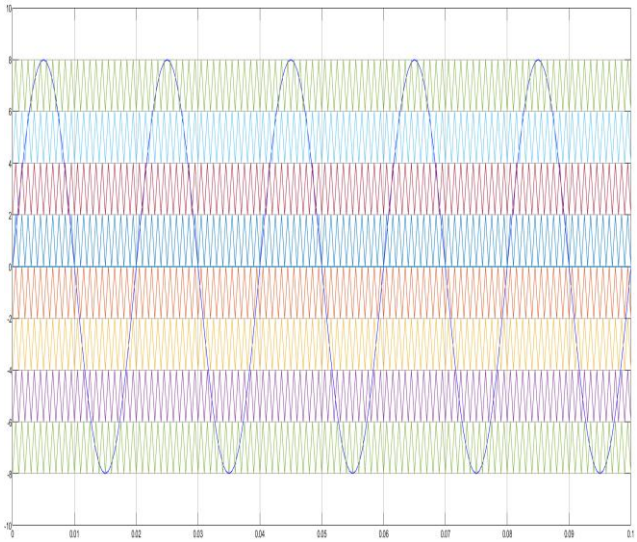

Fig: 2 PD Sinusoidal PWM technique

The regulation of an inverter with regard to its voltage and current is carried out using pulse width modulation techniques. The phase disposition PWM control scheme is used in proposed hybrid multilevel inverter. All carrier signals are in phase with one another both above and below the reference position value of zero. The upper four carrier waves are utilized to produce the positive signal, while the bottom four carrier waves are used to produce the negative peak of the inverter. A sine wave is used as the reference signal. Since there are eight carrier signals in this case, nine levels are generated (N= n+1), where N is the number of levels and n is the carrier signals. The utilization of eight carrier signals results the nine output voltage levels. Triangular waveforms with a carrier frequency of 1 kHz constitute the carrier signal. The carrier waveforms are built in the shape of phase arrangement. The sine wave with a frequency of 50 Hz is used as the benchmark. According to the change in the carrier signal, an AC waveform is generated.

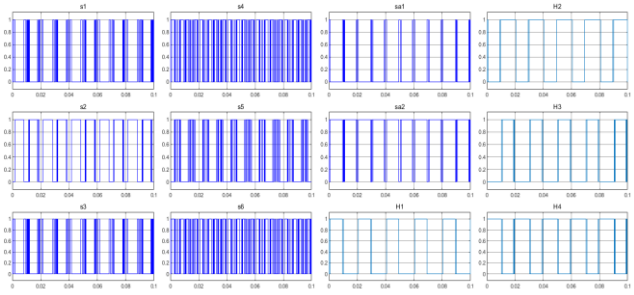

Fig: 3 Control signals

If the carrier signal's value is higher than the zero reference, it is represented as c + k (t) (k = 1, 2), and if it is lower, it is denoted as c k (t) (k = 1). Comparator compares and outputs "k" when reference signal value is greater than carrier c + k (t); otherwise, it outputs "k 1."When the reference value rises over the carrier's c k (t), the comparator compares both and outputs "(k 1)" otherwise, it outputs "k." By combining the acquired signals, a(t), an aggregated signal, is produced. The

output of the comparator is delivered to the switches in accordance with the level after comparing signal a(t) with constant required voltage levels.

IV. OUTPUT VOLTAGE WAVEFORMS AND TOTAL HARMONIC DISTORTION (THD)

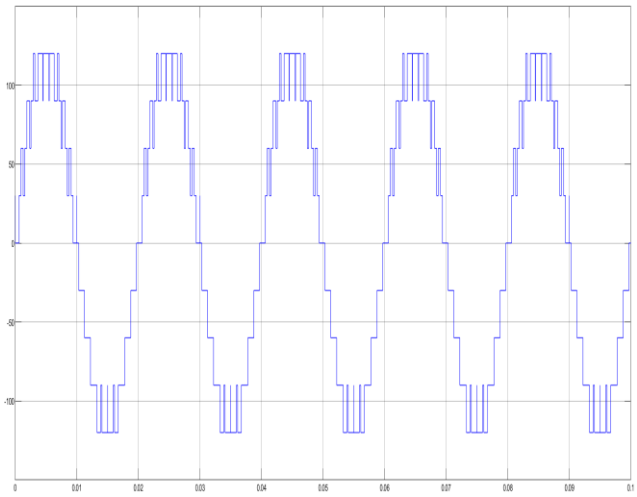

Fig: 4 Output Voltage Waveforms

Fig. 4 shows the output waveforms of a single phase, nine level hybrid MLI with a 50 Hz fundamental frequency. Using a symmetrical arrangement of the phase disposition carrier method, the proposed topology's output voltage is demonstrated. Based on switching frequency of 1 kHz and modulation index 1, the resistive load generates the nine level output voltage.

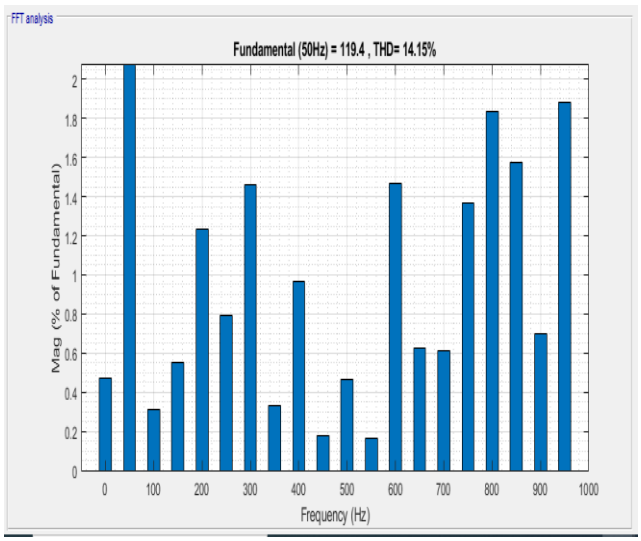

Fig:5 Output Voltage THD

According to Fig. 5, the output voltage's overall harmonic distortion is 14.15 percent. A 50Hz fundamental frequency is used to create the harmonics, which are then sampled at a Nyquist frequency. The harmonic order is indicated at the x-axis, while the harmonic magnitude is indicated at the y-axis.

Table: I Comparative analysis between previous work and proposed work

Topology	F_f	F_s	No: of Switches	Number of Output levels	%THD
Previous Work	50	1 KHz	12	7	15.5
Proposed Work	50	1 KHz	12	9	14.15

In this table. The two proposed works are contrasted with earlier research on hybrid MLI. The designed model is being examined using traditional topology in relation to the quantity of devices, output voltage ranges, and THD. The data clearly shows that the proposed topology generates nine levels at the output when the same number of components are used, which lowers THD levels as well.

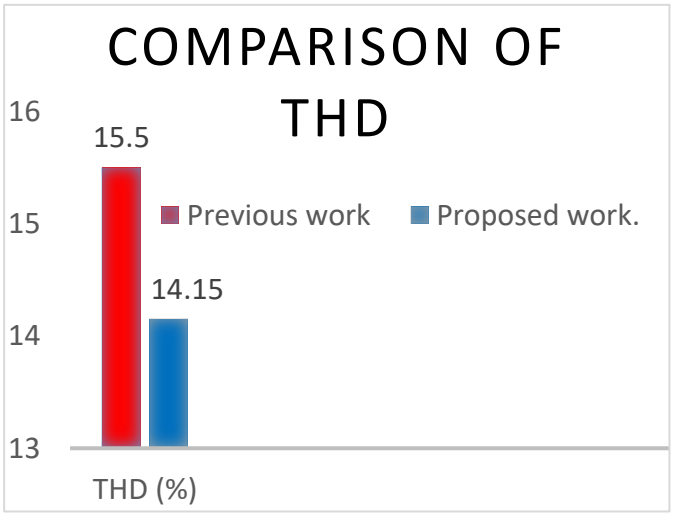

Fig: 6 Comparison of THD

The THD value of the suggested hybrid MLI is clearly lower than that of earlier work, as can be shown in fig. 6. A smaller filter is needed when THD is lower.

V. CONCLUSION

In this research work, a new single-phase hybrid MLI is proposed with a symmetrical configuration. A new topology is introduced with PD level shifted multicarrier switching scheme to produce nine level at the output voltage waveform, the main concern is to reduce the amount of power switches and input DC sources. Analysis of the suggested topology reveals that it requires significantly fewer power switches and has less complicated gate driver circuitry when compared to standard designs. With the functioning of many dc voltage sources in series and parallel, this offers sufficient flexibility for larger voltage and power requirements. The THD value of proposed hybrid MLI is lower than previous work done, lower THD results in smaller filter requirement. It is also observed that the levels at the output increases, THD decreases. The switched DC architecture is quite promising, according to the

scientific method based on losses and switch cost. Where isolated DC sources are convenient and can handle an inductive load, the proposed topology can be successfully implemented. Up to a certain point, the number of devices can be decreased.

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