International Journal of Electrical Engineering & Emerging Technology, Vol. 06, No. 01, JUN 2023, pp 1-7

Simulation and Evaluation of Cross Switched CT type Multilevel Inverter

[a]Noor Ul Ain, [b]Abdul Basit, [c]Wahib Khalid
[a,b,c] University of Engineering and Technology
Corresponding author e-mail: (noorulaink99@gmail.com)
[**Received on:** 11/05/2023 **Accepted on:**: 07/06/2023 **Published on:** 21/06/2023]

***Abstract* — A multilevel inverter is being used in modern power systems to make electricity reliable and stable. On the other hand, traditional multilevel inverters have disadvantages as well. This paper evaluates CT type cross switch multilevel inverters using eight switches. Implementation of cross switch is by connecting CT type back-to-back with the help of cross switches. This configuration can be used for both asymmetric and symmetric. The performance is evaluated by Phase disposition (PD) technique. This configuration has reduced THD while having high efficiency in comparison to other techniques. Execution of the model is on MATLAB/Simulink.**

***Index Terms* — CT, MLI, PD, MATLAB, Simulink.**

I. INTRODUCTION

MULTILEVEL inverters are most well liked and one of the most widely used inverters in power electronics (PE). These MLI are being utilized with different category capacitors, diodes semiconductor switches, and DC supplies. This configuration can produce distinct voltage levels. MLI these characteristics has made it appealing in medium to high power system applications.

The MLI in comparison to a traditional inverter has many advantages which includes reduction in harmonics, high voltage levels, and less total harmonic distortion. Traditional MLI are distinguished into three types of Cascaded H-bridge (CHB), neutral point clamp (NPC) and flying capacitor (FC). Among the three categories CHB is in demand as it does not have the drawback of the remaining two. The main disadvantage of FC and NPC is usage of more capacitors, high switching losses and distorted DC voltage. These issues were less in CHB.

A multilevel inverter model in [4] has been given which is having less PE equipment. But passive components utilized is more making it less efficient. Another approach of researcher in [5] implemented a topology with less switches and obtained more number of voltage levels with asymmetrical arrangement. Though it achieved higher voltage level with less number of components but the basic purpose of MLI was violated because of switches which utilizes high voltage.

The conventional MLI can merge to develop hybrid MLI and produce increased voltages. These MLI fall under the asymmetric category. To expand the number of voltage levels with electronic components that consume less power, asymmetric MLI employs several dc voltage levels.. This topology can increase voltage levels exceptionally, but it disobeys the aim of designing switches with less voltage ratings for applications having high power consumption.

The configuration of CT-type MLI proposed in this paper is using MOSFETs (semiconductor switches) to produce maximum level of voltages ensuring high quality voltage. Also keeping in concern of minimum power component usage in the model making it economical. The design of the topology utilizes two T-type modules connected back-to-back to integrate nine level output. The key benefit of CT type switch is that it does not utilize extra power components to integrate negative voltage levels. The configuration has eight semiconductor switches along with four equal dc link sources. The output has four positive, four negative and one zero level. This approach reduces complexity as well as voltage stress and works without self-balancing.

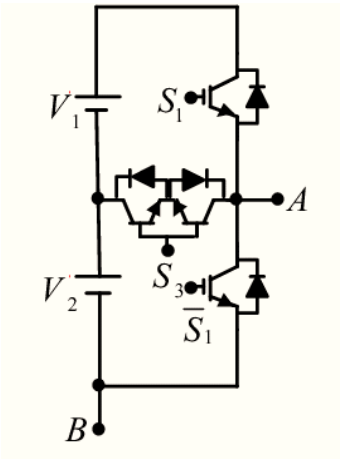


Figure 1 T type module

II. FUNDAMENTAL OPERATING OF CT-TYPE MLI

A. Module Configuration

The fundamental T-type module establishes the CT type configuration. In two T-type modules each consist of two semiconductor switches with unidirectional, one bidirectional and two dc link sources. By obstructing bidirectional current,

the bidirectional switch limits the short circuit of dc sources, as depicted in Fig.1. Fundamental module can generate three level voltage output. The output can be measured at point A.

The proposed CT- type module is a combination of two T modules connected back-to-back. Two switches that have been crossed-connected create this arrangement. L and R refer to the two T type modules, respectively. There are three points in the modules: A, B, and C. From point A and L to point C and R, there are switches that are cross connected. Both modules' outputs are connected at locations B. By lowering power elements, the arrangement can generate distinct voltage levels. More voltage levels are expected to significantly minimize THD with lower switching frequency.

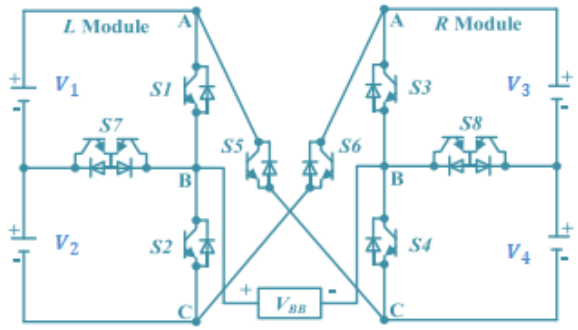


Figure 1 Proposed CT-type multilevel inverter

B. Fundamental Working of MLI

The CT type arrangement comprises ten MOSFETs with four dc supplies along with diodes as shown in fig 2. This configuration produces a nine level output voltage of equal magnitude with dc sources. Setting up various pathways for current from DC sources is the main concept behind this design. As the dc sources of the L and r modules are coupled in a fashion that provides negative voltage, preventing cross-switches from operating concurrently, this design does not use an H bridge. The cross-connected switches S5, S6, and the adjacent switches S1, S2, S3, and S4 are unidirectional. The L and R modules' central semiconductor switches can operate in either direction. The dc supply has the same magnitude since the setup is symmetric (V1=V2=V3=V4=E). The switching order is chosen in a way that prevents the anode of diodes from being linked to the positive of the dc supply in order to conduct current. Moreover, adding a benefit as different switching components utilizes the same polar level in CT-type MLI making it self-balancing MLI. The semiconductor switches connected side by side can't operate simultaneously. This type of configuration is beneficial in space vector modulation as it requires minimum switching which reduces losses.

C. Development of Simulation Model of Proposed Topology

The Configuration proposed is executed on Simulink. The design consists of two bidirectional and six unidirectional semiconductor switches with four dc supplies. The voltage level output can be increased by increasing symmetrical dc supplies. The voltage level can be calculated by the following equation:

$$N = 2n + 1 \qquad (1)$$

And maximum voltage gain can be calculated by:

$$V_m = n \times V_{dc} \qquad (2)$$

Where N is the number of levels, and n is the number of dc supplies.

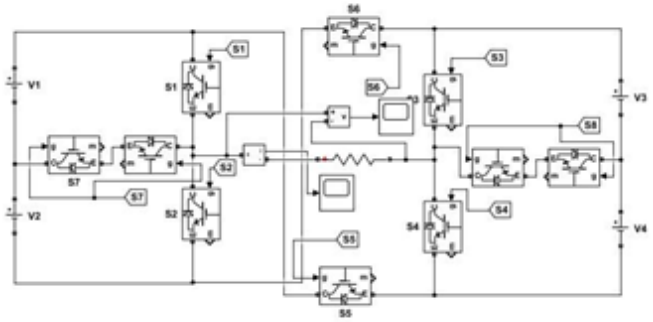


Figure 2(a) CT type model on MATLAB Simulink

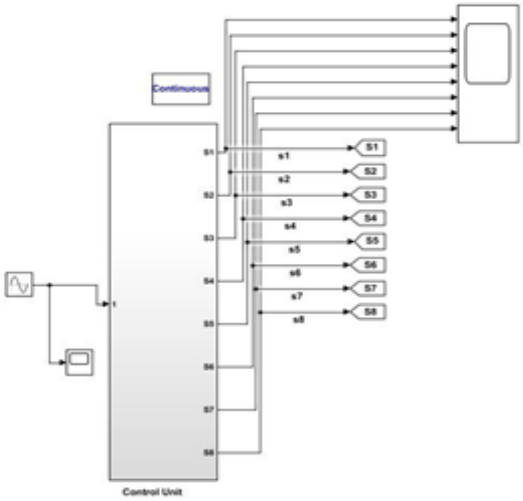


Figure 3(b) Proposed topology of control system

Table 1 Symmetrical switching operation table

Modes	**Modes of the various states of switching**							
V_{BB}	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**
4E	✓	×	×	✓	×	✓	×	×
3E (a)	✓	×	×	×	×	✓	×	✓
3E (b)	×	×	×	✓	×	✓	✓	×
2E (a)	✓	×	✓	×	×	✓	×	×

2E (b)	×	✓	×	✓	×	✓	×	×
2E (c)	×	×	×	×	×	✓	✓	✓
E (a)	×	×	✓	×	×	✓	✓	×
V_{BB}	**S_1**	**S_2**	**S_3**	**S_4**	**S_5**	**S_6**	**S_7**	**S_8**
E(b)	×	✓	×	×	×	✓	×	✓
0 (a)	×	✓	✓	×	×	✓	×	×
0 (b)	×	✓	×	✓	✓	×	×	×
-E (a)	×	×	×	✓	✓	×	✓	×
- E (b)	✓	×	×	×	✓	×	×	✓
-2E(a)	×	×	×	×	✓	×	✓	✓
-2E(b)	×	✓	×	✓	✓	×	×	×
-2E (c)	✓	×	✓	×	✓	×	×	×
-3E (a)	×	✓	×	×	✓	×	×	✓
-3E (b)	×	×	✓	×	✓	×	✓	×
-4 E	×	✓	✓	×	✓	×	×	×

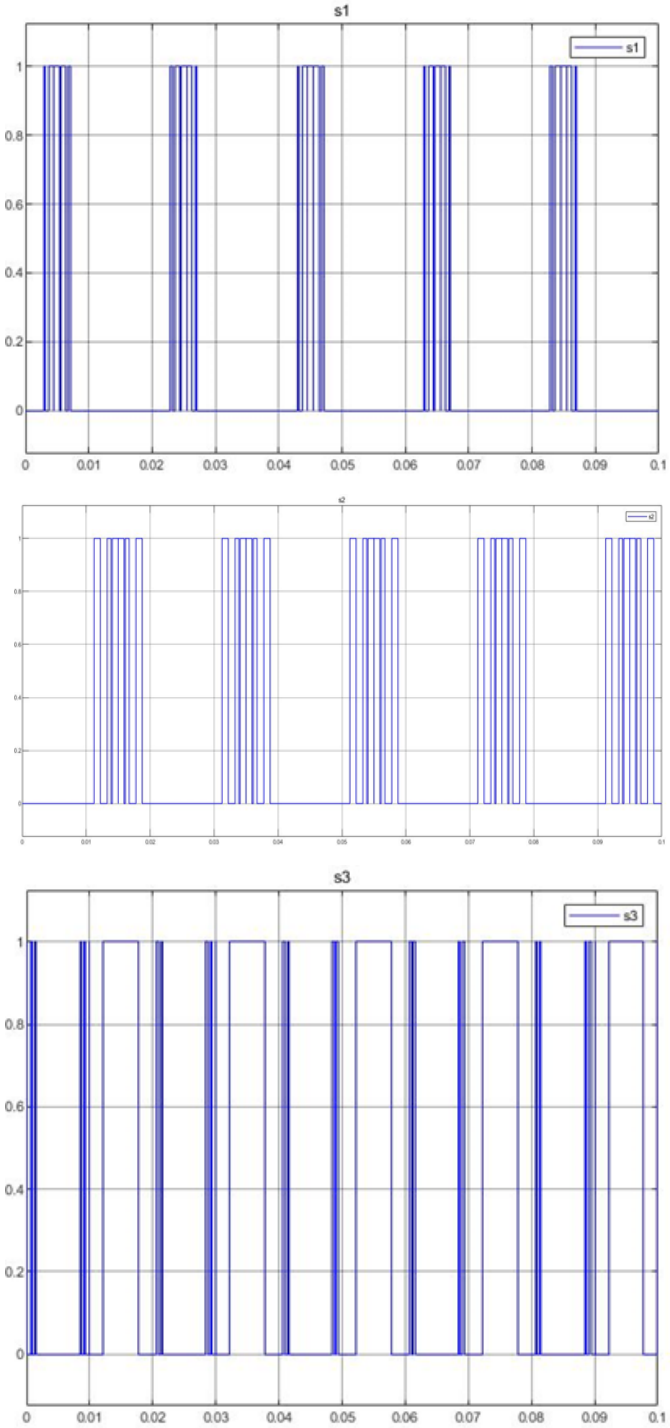
III. CONTROL TECHNIQUE

For controlling switching of multilevel inverters are divided into two types on the basis of frequency as low frequency modulation and high frequency modulation. Pulse width modulation is a high frequency modulation technique that is further classified into phase disposition (PD-PWM), phase opposition disposition (POD-PWM) and alternative phase opposition disposition (APOD-PWM). for the proposed model of CT- type multilevel inverter phase disposition technique is utilized. These level shift PWM techniques N-1 carrier signals are used which are vertically shifted. it produces N number of levels.

Phase Disposition technique:

The number of carriers utilized are eight to produce 9 level output. The proposed symmetrical model PD-PWM control technique is used to produce nine levels. This scheme is used to have a desirable harmonic spectrum. Every carrier signal has one kilohertz frequency with the reference signal having fifty Hertz frequency. Comparison of carrier signal is made with reference signal as per requirement of switching scheme PD-PWM. In the PD technique all switching signals are in phase.

This scheme is performed on MATLAB Simulink to produce nine level output voltage. Switching order is shown in fig below.



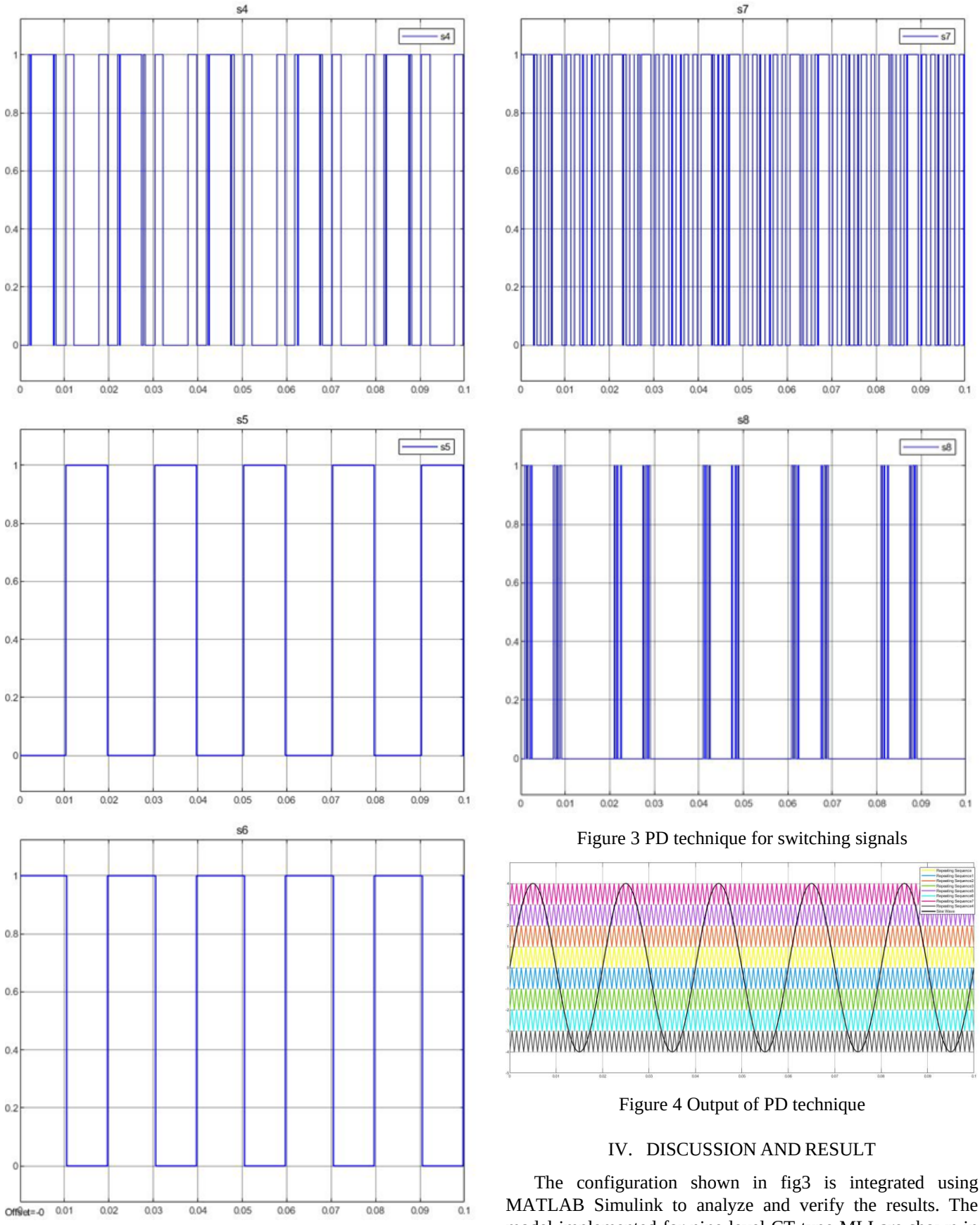


Figure 3 PD technique for switching signals

Figure 4 Output of PD technique

IV. DISCUSSION AND RESULT

The configuration shown in fig3 is integrated using MATLAB Simulink to analyze and verify the results. The model implemented for nine level CT type MLI are shown in figure 6. The FFT analysis of the harmonic spectrum is analyzed of output waveforms as shown in fig 7 and 8. As the

source voltage for L and R are the same, each step size is also equal (step size=10V). The voltage obtained in output is 40V maximum.. This voltage output confirms high performance of the model. Total harmonic distortion (THD) of the model after control scheme PD is 14.40% and THD of current is 0.16% as shown in fig 8. After implementation of PD control technique the THD has decreased to great extend while reducing the complexity as well.

Table 2 Variables of CT type model

Configuration	**Voltage Output**	**V1=V2=V3=V4=E**	**Frequency**	**Resistor**
Symmetric	40V	10V	1KHz	10ohms

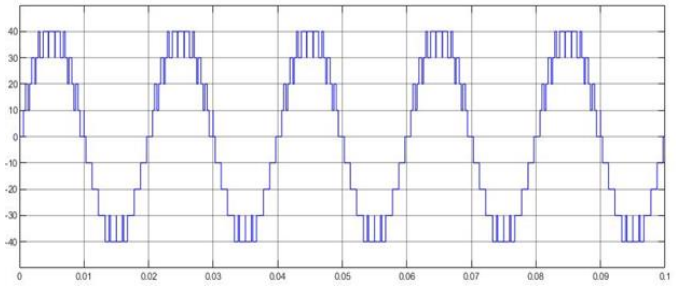


Figure6 Output of CT type nine level model

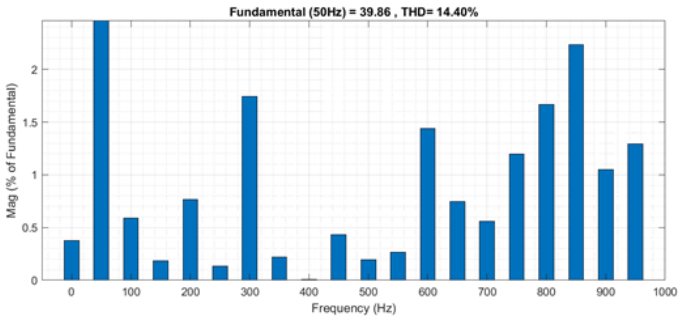


Figure 7 FFT voltage output of CT type converter

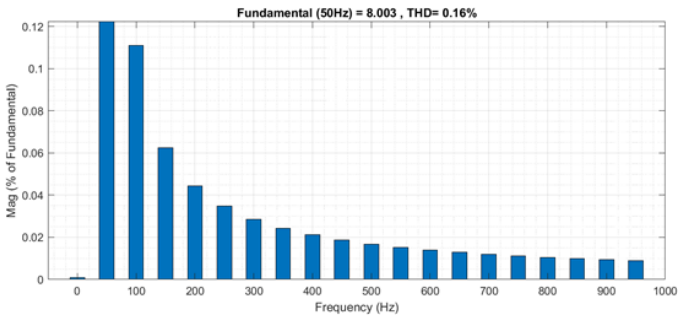


Figure 5 FFT current output of CT type converter

V. CONCLUSION

This paper presents a novel model of MLI that generates high voltage output levels namely CT-type multilevel inverter. The configuration is highly ordered and can be utilized in high and medium applications smoothly. One of the benefits of the design is that it reduces complexity and reliability of the system is improved. As negative voltage levels are also produced by the same configuration without using H-bridge. The design can be extended easily to have more output voltage levels. The THD of the system is also reduced as shown in result 14.40%. Switching redundancies is introduced by symmetrical operation which is beneficent during power failure issues.

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